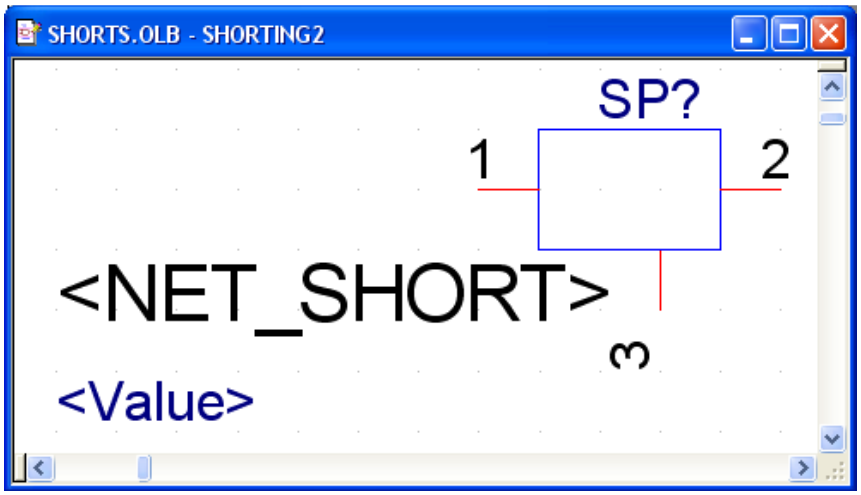
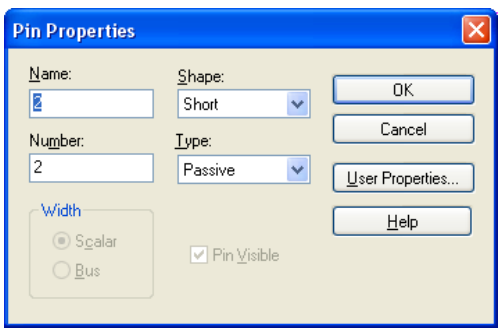
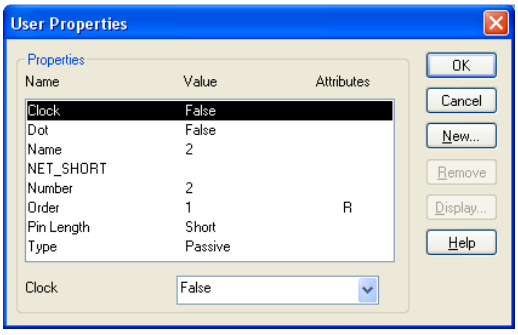
How to create a net short symbol in Capture and transfer it into PCB Editor

Open OrCAD Capture and create a new schematic symbol. The number of pins required relates to the number of nets you wish to short. For this example we are going to short three nets together.

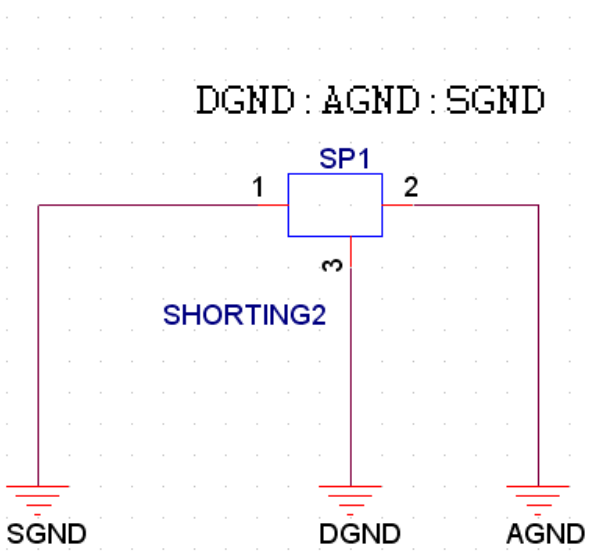


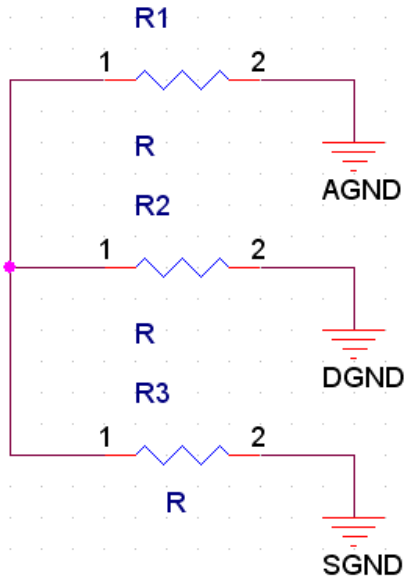
For each pin add a new user property called NET_SHORT with no value. On This example the property is also displayed so it can be viewed in the schematic.





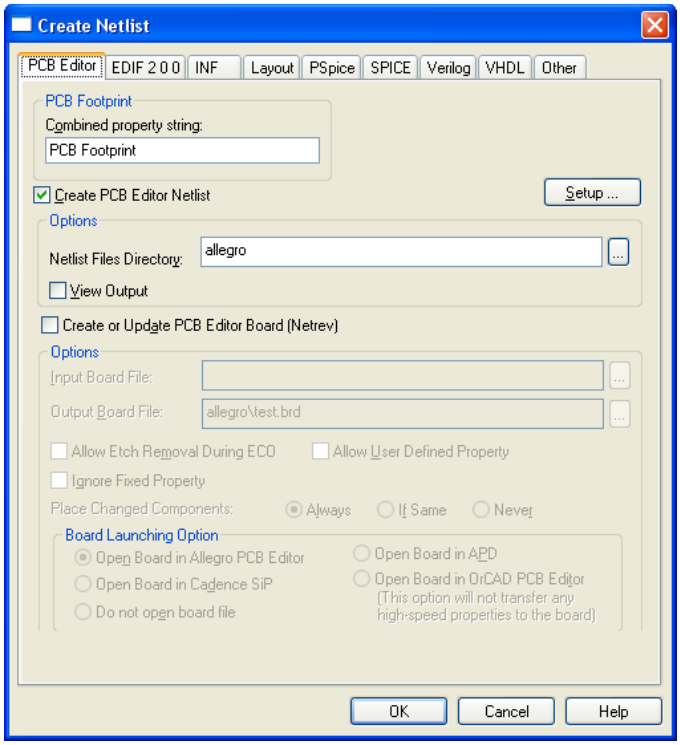
Save the symbol in a defauly company library. Draw your circuit using the new short symbol to logically define your net short locations on the schematic. Example shown below.



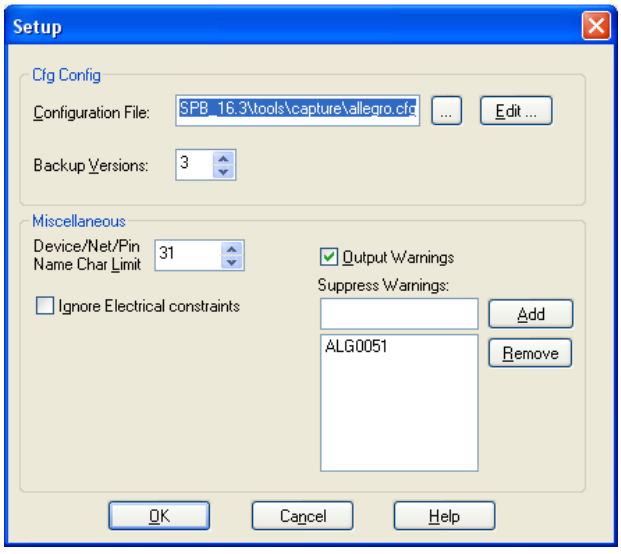


On each pin on the net short (SP1) you need to edit property and add the net names that you wish to short seperated by a colon. In this example the nets are DGND:AGND:SGND. You also need to ensure that you have a pcb footprint defined for this part.

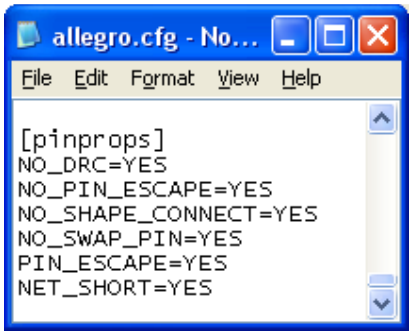
Next we create the netlist. We need to add a pin property to the allegro.cfg file to send the net short information into PCB Editor. To do this select the dsn file in the project window and then run Tools – Create netlist



Press the Setup button

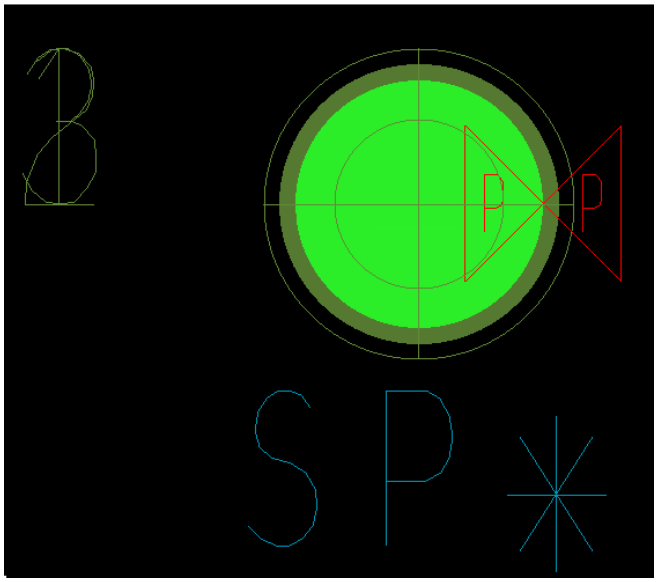


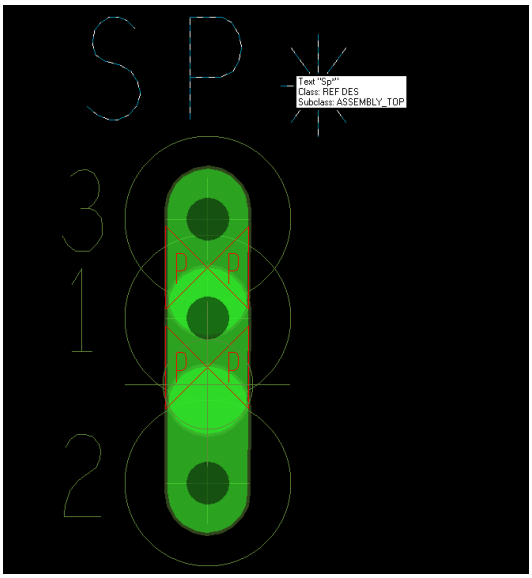
Next press the Edit button and add the following entry to the [pinprops] section. NET_SHORT=YES



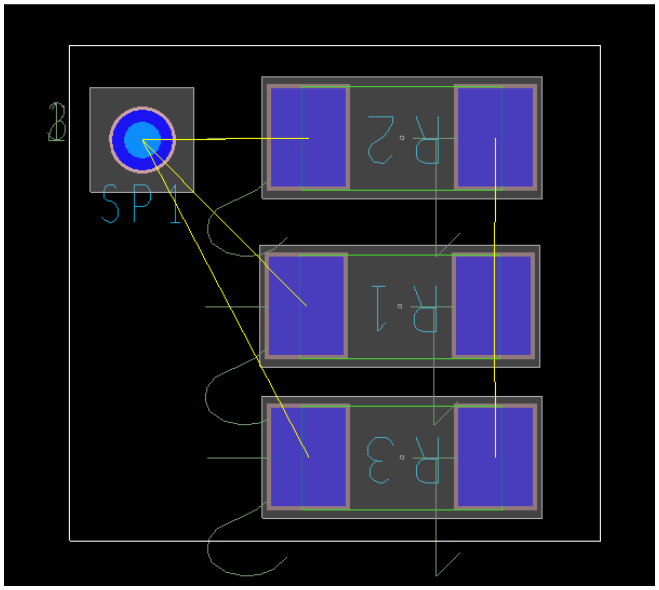
Save and close the allegro.cfg file.

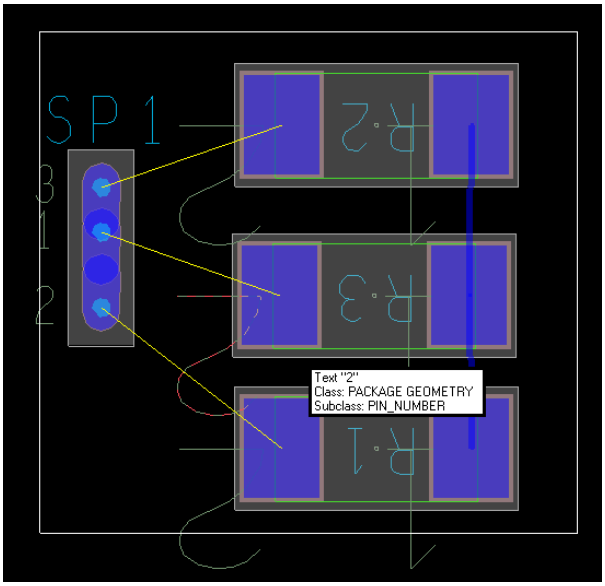
We can now create a net short footprint part for this schematic symbol. Open PCB Editor and create a new package symbol. For the footprint you have several options. You can either add three pins that use an oblong shaped pad which creates the short or just add three pads on top of each other. Both options are shown below as examples. You will get DRC's in the symbol mode, these will be corrected once the netlist is imported into the PCB.





Open the board file and import the netlist from Capture. Place your components. You will notice in the next screenshot that the net short SP1 is placed and there are no DRC errors.





There are advantages and disadvantages to either footprint, the first uses less real estate but you will still get some DRC's if the three connections are routed on the same layer (ideal for multi-layer boards). You will not get these DRC's if you use the second option but it does take up more real estate.

The final view below shows a show element view of one of the net short pins. You can see the NET_SHORT property applied to the pin.