cadence

RF Power Amplifier Design

Efficiently Defining the Fundamental and 2nd and 3rd Harmonics Load Impedances for Optimum “Antifragile” Performance

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Contents

Purpose

This application note describes how to determine simultaneously the fundamental and 2nd and 3rd harmonics load impedances of an RF/microwave transistor in non-linear operation by using an efficient procedure which produces optimum, robust, and antifragile[1] performance.

Audience

This document is intended for intermediate and advanced level AWR Design Environment users who are familiar with the program interface, creation of schematics and graphs, and interpretation of graphical output.

Overview

Defining the 2nd and 3rd harmonics load impedances of an RF/microwave transistor in non-linear operation is a strongly determining factor not only for the synthesis of the output matching but also for the simulation of load-pull power and efficiency contours on a Smith Chart.

This procedure will provide you in a straightforward way with the initial data to proceed to load-pull simulations with the 2nd and 3rd harmonics impedance properly defined. Many transistor data sheets today provide load-pull contours data without reference to the harmonics load impedances or if it is included no explanation is given for why the particular values are chosen.

Similarly, some transistor nonlinear models do not provide access to the voltage and current across the intrinsic generator where the harmonics impedances will define what Class of wave forming mode of operation such as Class-B, Class-F, Class-invF, Class-J, or other will be used.

There are many scientific articles and books on this subject that should be read and understood. Their use of complex mathematical expressions, however, do not provide a simple procedure to define the necessary fundamental load impedance with appropriate 2nd and 3rd harmonic load impedances for optimum performance and robustness to all possible tolerances, static or dynamic of the environments, without necessity to have a PhD degree.

Procedure with transistor model with access to the intrinsic generator

The following procedure describes how to determine the fundamental and 2nd and 3rd harmonics load impedances of an RF/microwave transistor when its non-linear model allows access to the nodes of intrinsic generator so that the voltages and currents can be measured.

These steps include creation of entire schematics, and graphs and measurements, as well as use of standard AWR Design Environment features such as tuning and sweeping. Detailed creation and use instructions are not provided for individual steps.

1. Create the schematic shown in Figure 1.:
    - Include your chosen transistor. In this case it is a 25W GaN HEMT.
    - Use an output tuner for the fundamental and the 2nd and 3rd harmonics frequences with default values.
    - Bias the drain current per the transistor data sheet.
    - Tune the input using linear simulation for a good input match and K-factor ≥ 1 to minimize the input power and distortion of input nonlinear effects at output.

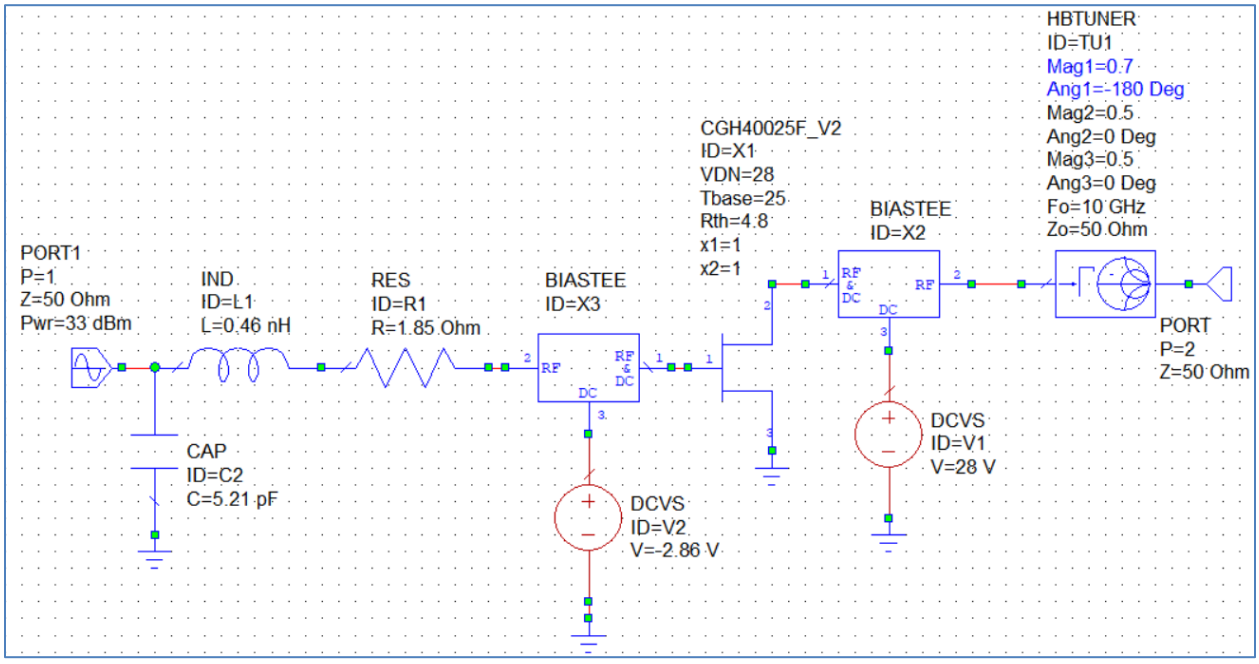


Figure 1

2. On the Options dialog box *APLAC Sim* tab for the CGH40025 stage schematic (Figure 2), specify `1` for *Tone 1 Harmonics* to use the fundamental frequency and no other harmonics for nonlinear harmonic balance simulations.

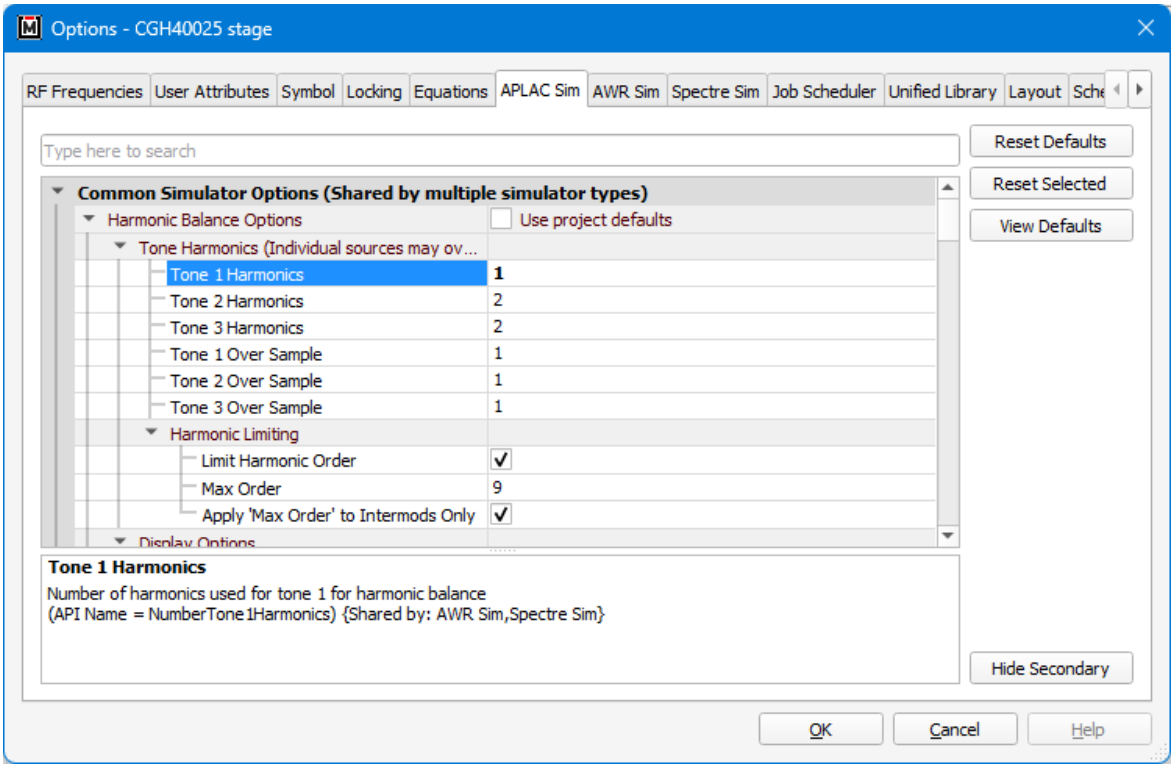


Figure 2

3. Add the schematic from Figure 3 to simulate the IV curves of the transistor.

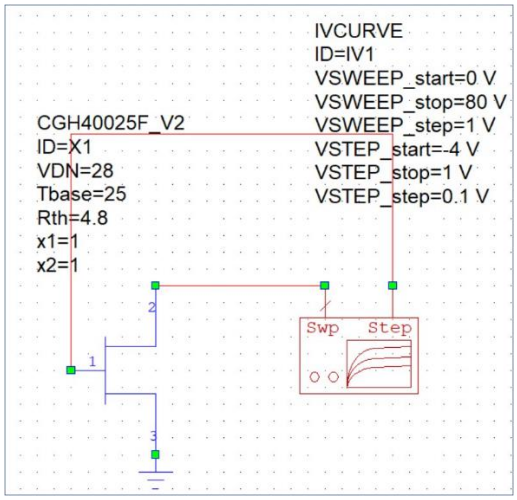
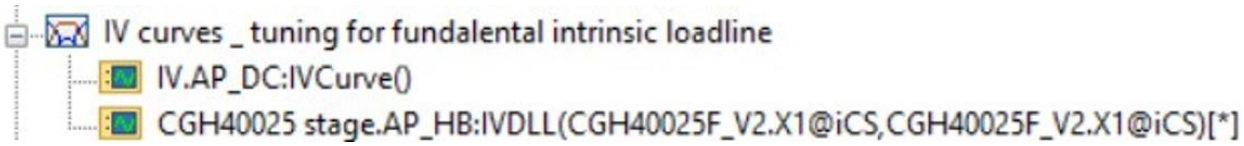


Figure 3

4. Add a graph with the following measurements.



The Figure 4 shows how to select the first measurement for the IV curves simulation.

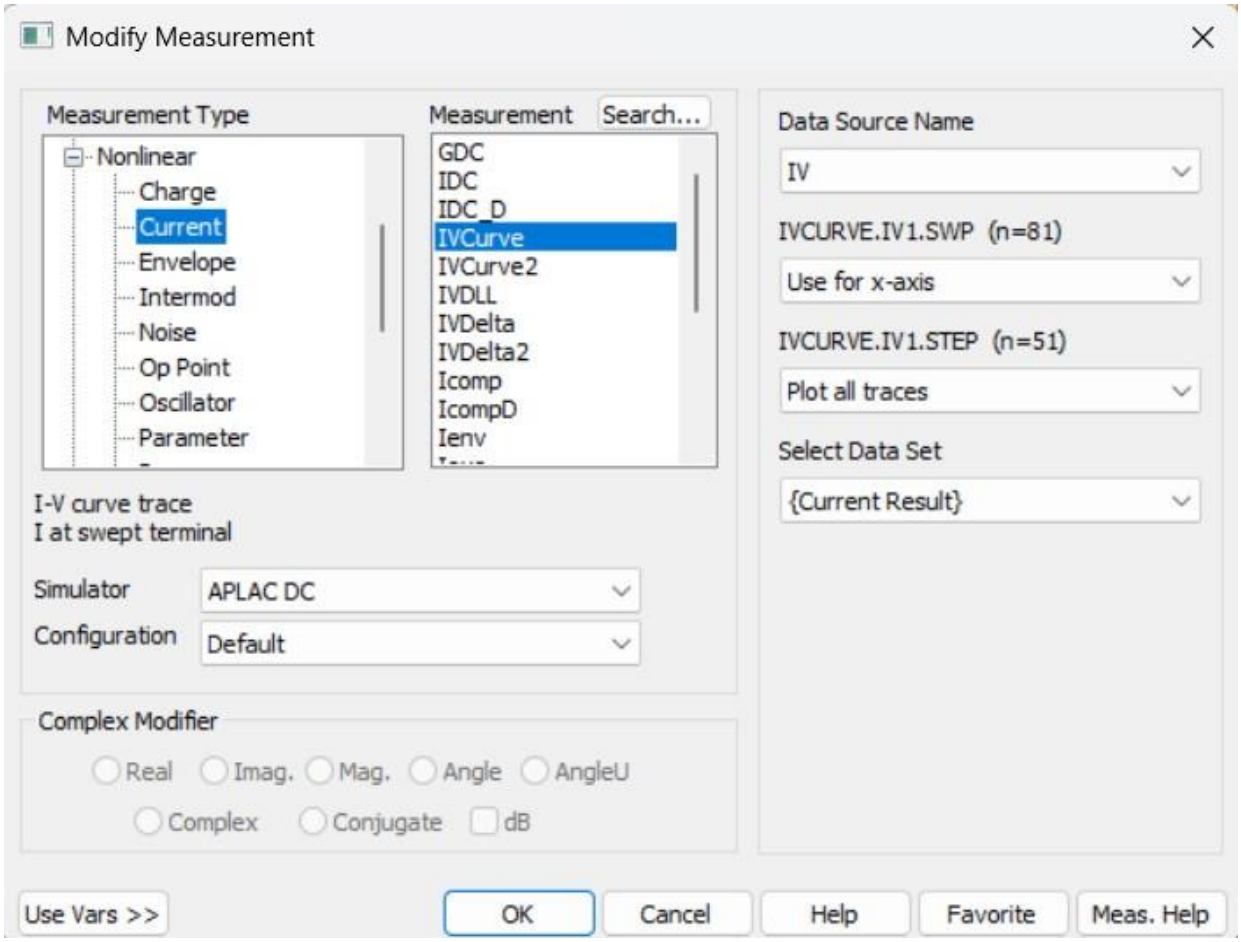


Figure 4

5. Add the second simulated measurement to plot the fundamental frequency load-line over the IV curves starting as per Figure 5.

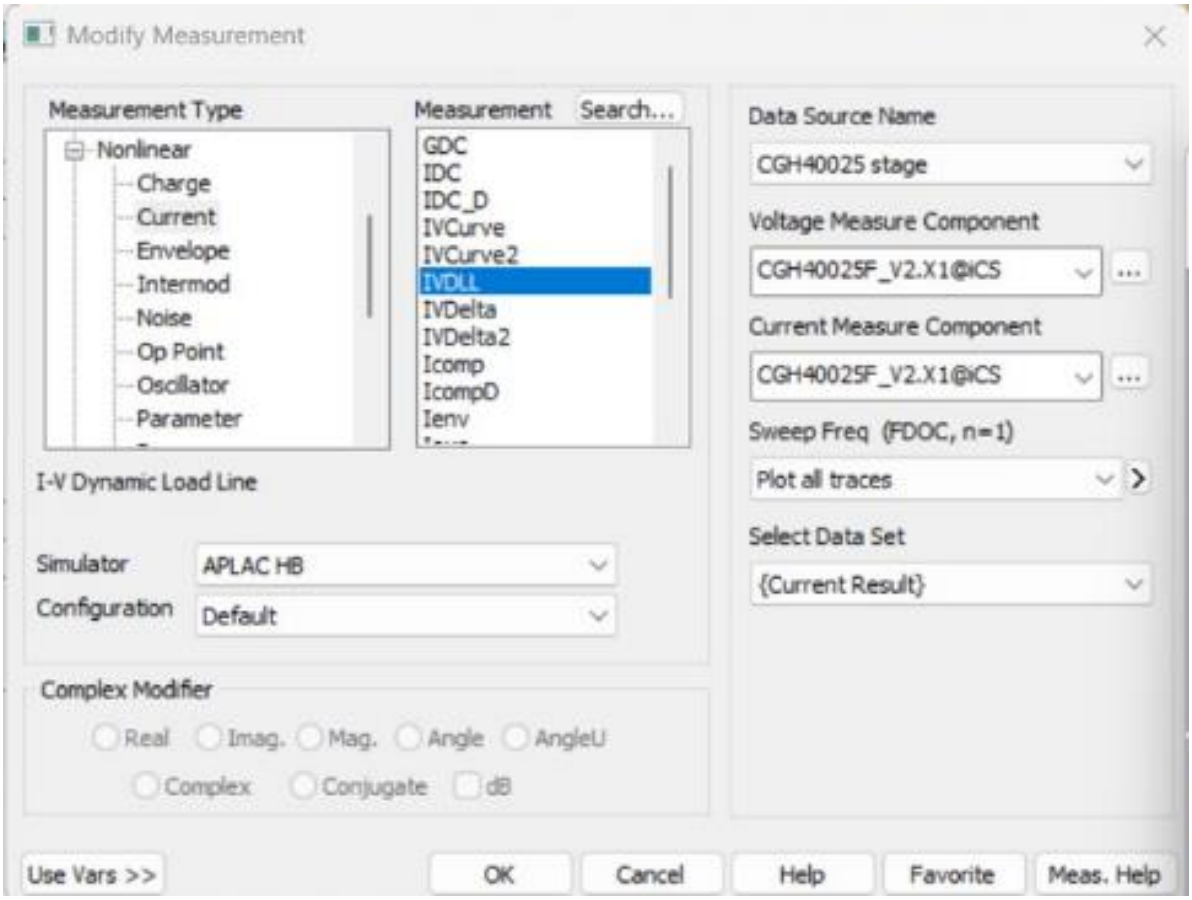


Figure 5

6. Click the ... button to open the selection window as per Figure 6, then select the "Drain-source branch" of the transistor model first for voltage and then for the current measurement. This fundamental load-line, a pure sinusoid, is formed by the voltage and current across the intrinsic generator of the transistor model.

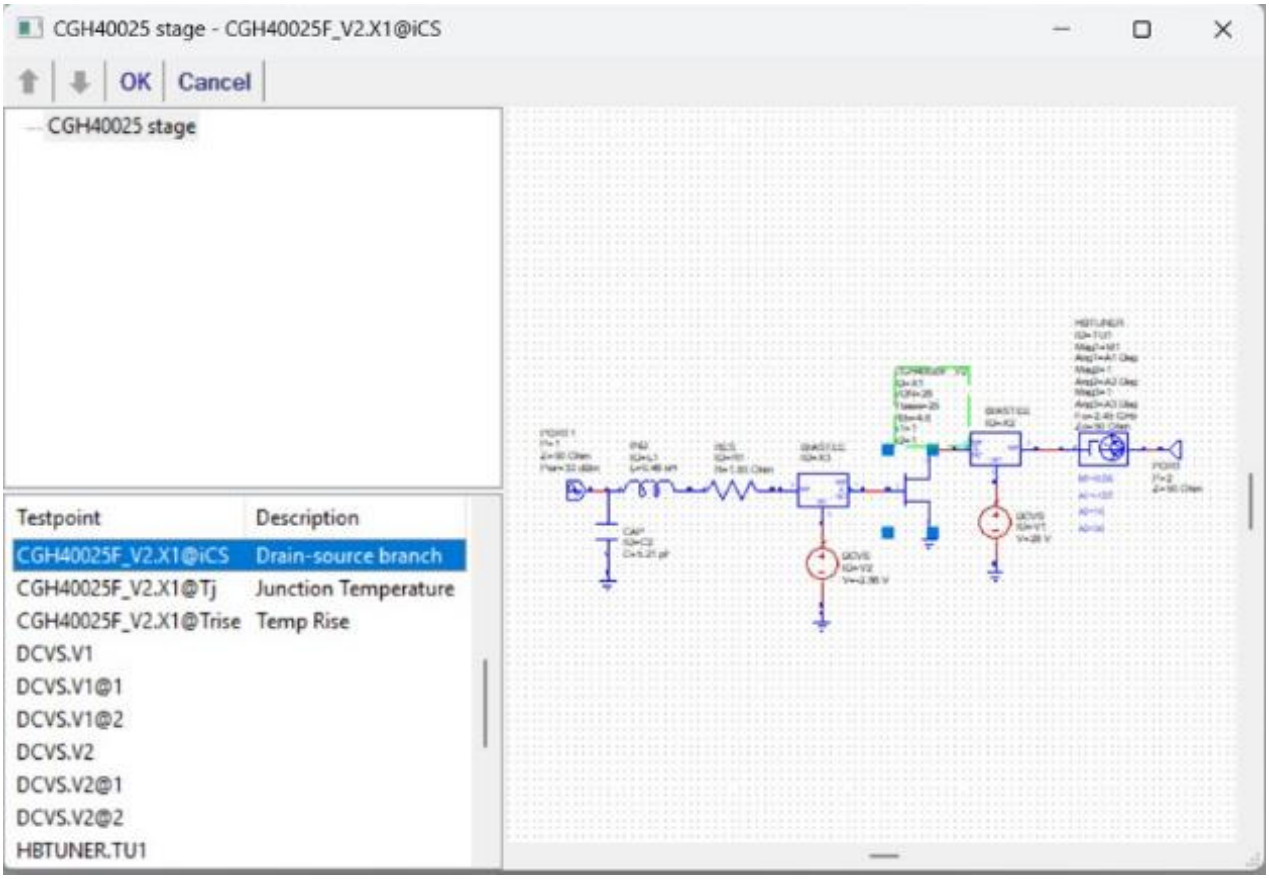


Figure 6

7. Using the Tuner, tune the fundamental frequency load-line as shown in the Figure 7, using enough power to expand it beyond the IV curves boundaries.

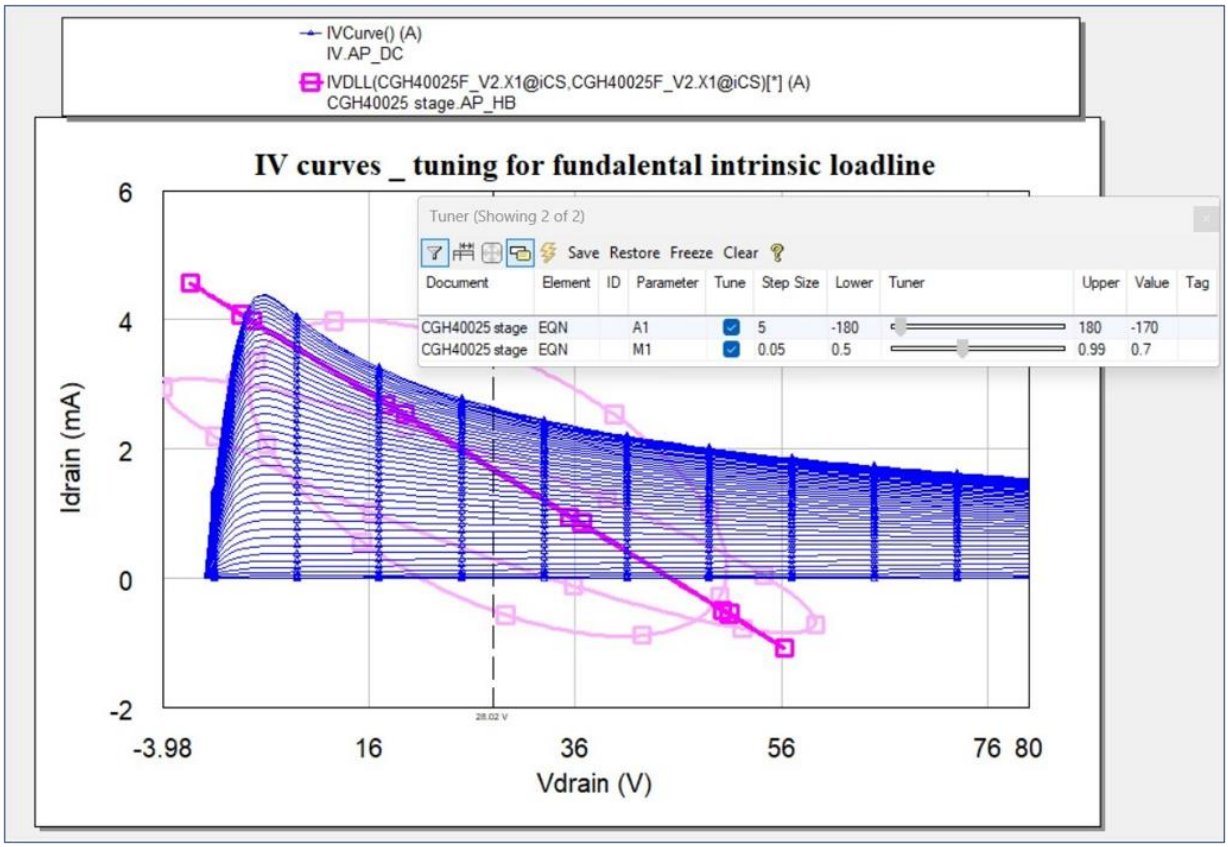


Figure 7

A load-line which looks like a single line represents a resistive-only load impedance to the intrinsic generator with the values of reactive parasitic elements tuned out. It is positioned approximately to provide maximum RF voltage and current swing and in this way maximum RF output power.

Notice that the fundamental load-line extends beyond the boundaries of IV curves.

8. Increase the harmonic tones to 3, simulate to get the result of Figure 8 which shows the complex load-line formed by the tones of the fundamental and 2nd and 3rd harmonic frequencies.

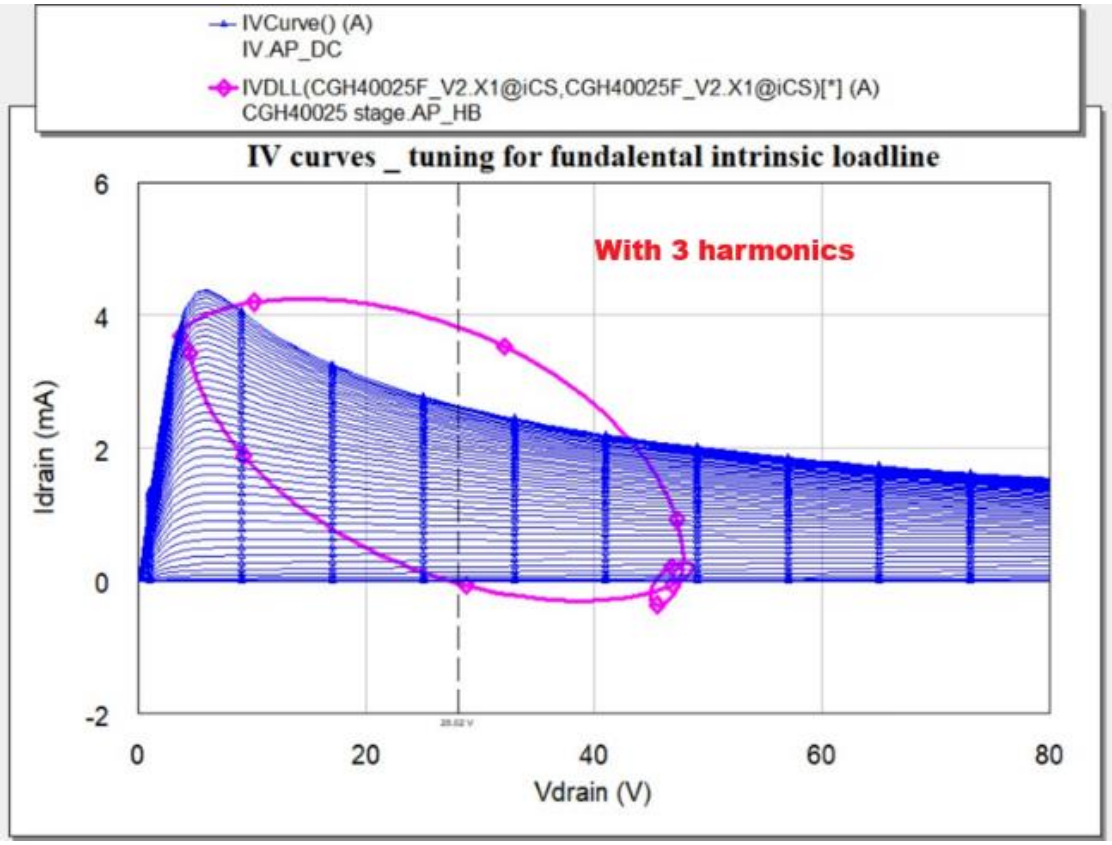


Figure 8

9. Then increase the tones to 15 to get the result of Figure 9. Now the complex load-line is fully contained by the boundaries of the IV curves.

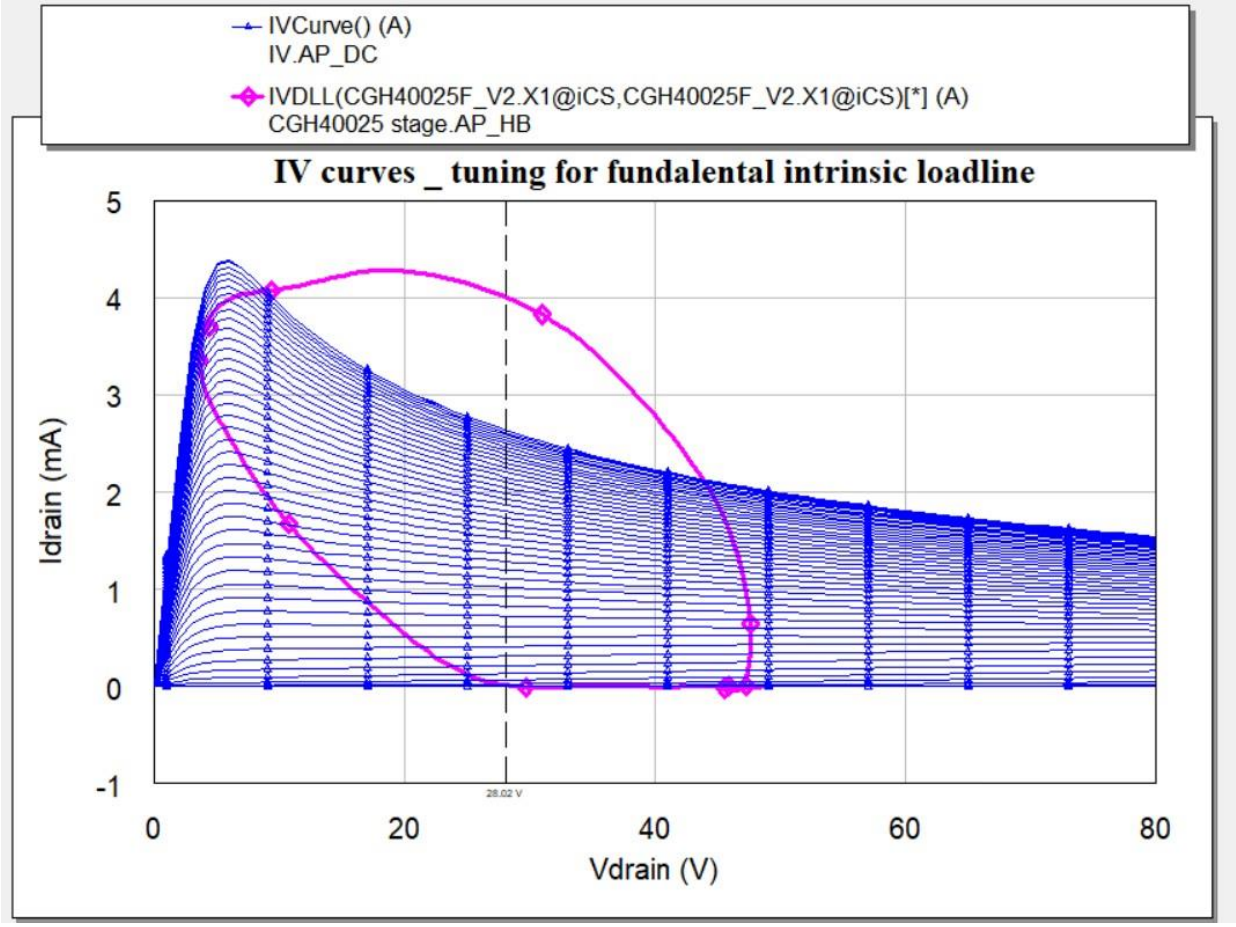


Figure 9

10. Go back to 3 tones and simulate using the following equations to present the intrinsic fundamental and 2nd and 3rd harmonic impedances on the Smith Chart a at the reference plane of the intrinsic generator.

```
Igen = CGH40025_stage.AP_HB:Icomp(CGH40025F_V2.X1@iCS,1)
Vgen = CGH40025_stage.AP_HB:Vcomp(CGH40025F_V2.X1@iCS,1)

Zintr=(-Vgen/Igen)
Gama_intr=(Zintr-50)/(Zintr+50)



Igen2 = CGH40025_stage.AP_HB:Icomp(CGH40025F_V2.X1@iCS,2)
Vgen2 = CGH40025_stage.AP_HB:Vcomp(CGH40025F_V2.X1@iCS,2)

Zintr2=(-Vgen2/Igen2)

Gama_intr2=(Zintr2-50)/(Zintr2+50)


Igen3 = CGH40025_stage.AP_HB:Icomp(CGH40025F_V2.X1@iCS,3)
Vgen3 = CGH40025_stage.AP_HB:Vcomp(CGH40025F_V2.X1@iCS,3)

Zintr3=(-Vgen3/Igen3)

Gama_intr3=(Zintr3-50)/(Zintr3+50)
```

11. In Figure 10, looking at the Smith Chart, tune the 2nd and 3rd harmonic intrinsic impedances to be a short circuit as it is shown.

    Pout, drain and power added efficiencies and gain @ Pout are shown in the graph on the right in Figure 10

    This is a Class-B operation and probably close to max Pout for the 25W transistor. Trying to tune the fundamental intrinsic impedance for maximum performance produces only 0.1dBm better power in this case.

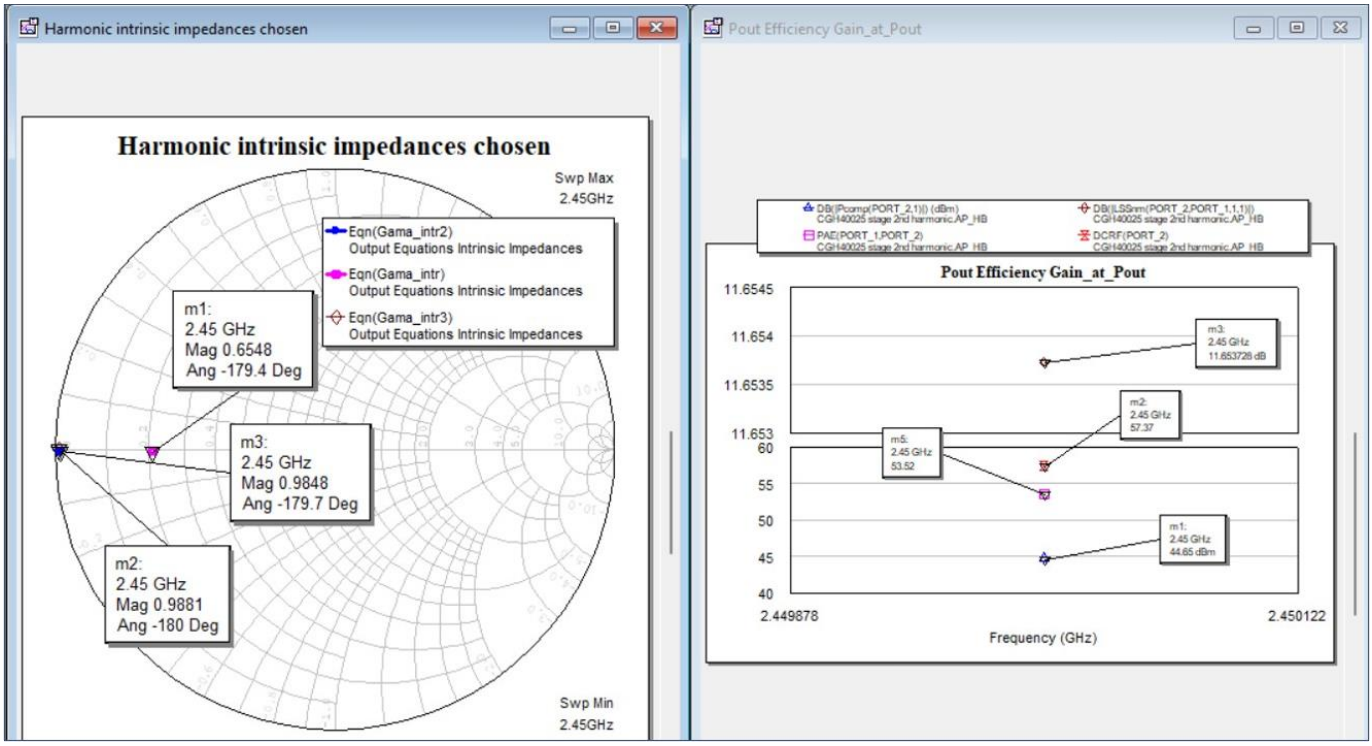


Figure 10

12. In the schematic of Figure 11, where the output tuner is with values for Class B, add a sweeping variable for the 2nd harmonic angle in the tuner (Ang2) to be swept across the outskirt of the Smith Chart with 5-degree steps. The magnitude should be 1, which means full reflection and simulate.

    In a duplicate schematic do the same for the 3rd harmonic reflection coefficient (impedance).

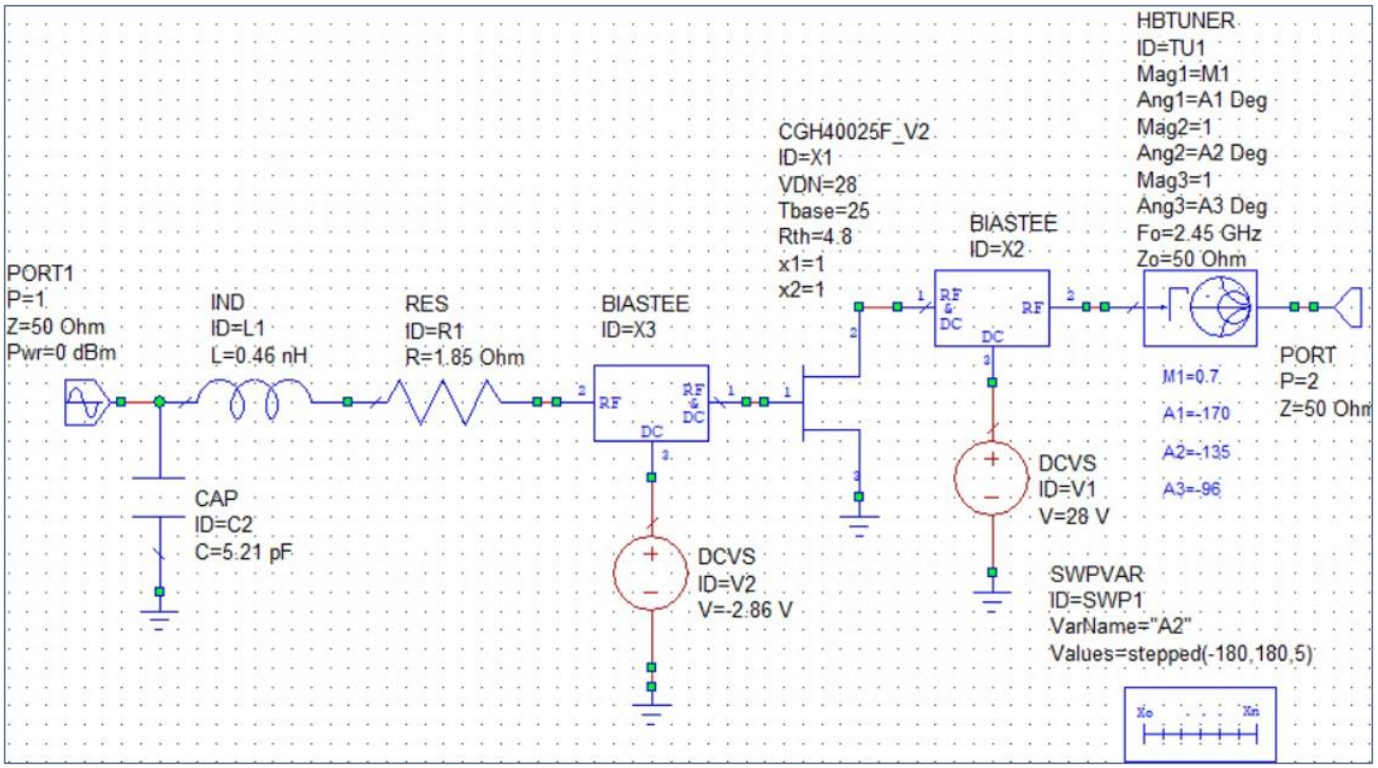


Figure 11

An Observation

In the following Figures 12 and 13, the 72 5-degree steps of the angle of the harmonic reflection coefficients at the drain outside terminal are concentrated in a small area at the intrinsic generator. It should be obviously that the condensed area is due to the output capacitor C_{DS} of the transistor.

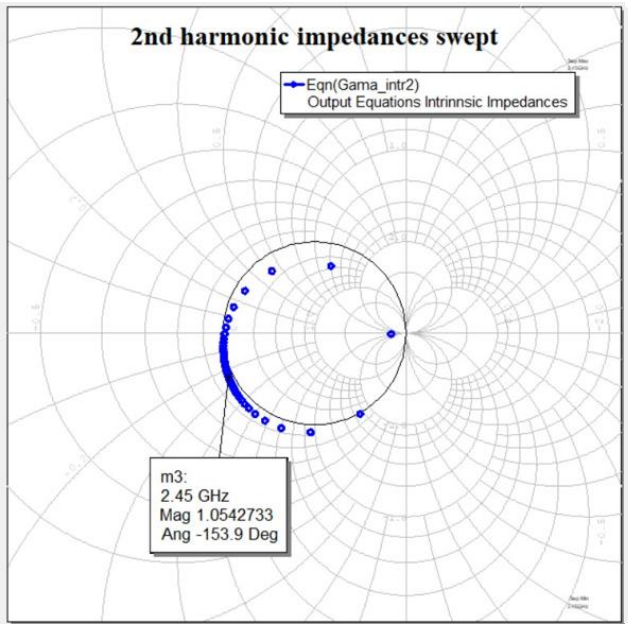


Figure 12

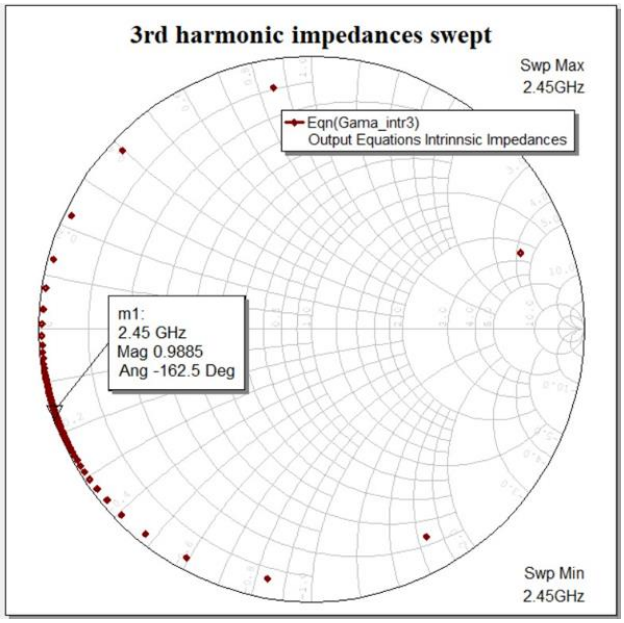


Figure 13

Note that the second harmonic intrinsic impedance exhibits a negative resistance in some areas. This may seem unusual, but it is a real and known parametric effect for nonlinear capacitors[4]. The effect at the intrinsic generator is from both C_{GS} and C_{DS}. In most models the C_{DS} is not modelled as nonlinear, but with a constant value, and this effect is not strong in simulations. In practice, it has a strong effect which is well modelled with nonlinear C_{DS} for the transistor models of Cree (now MACOM).

If the effect of a negative resistance in the harmonic intrinsic load is much stronger, tuning the fundamental intrinsic load to exhibit a capacitive reactance as in Figure 14 dampens the effect. However, if the excursion into negative resistance is small there is rarely a need to use this technique.

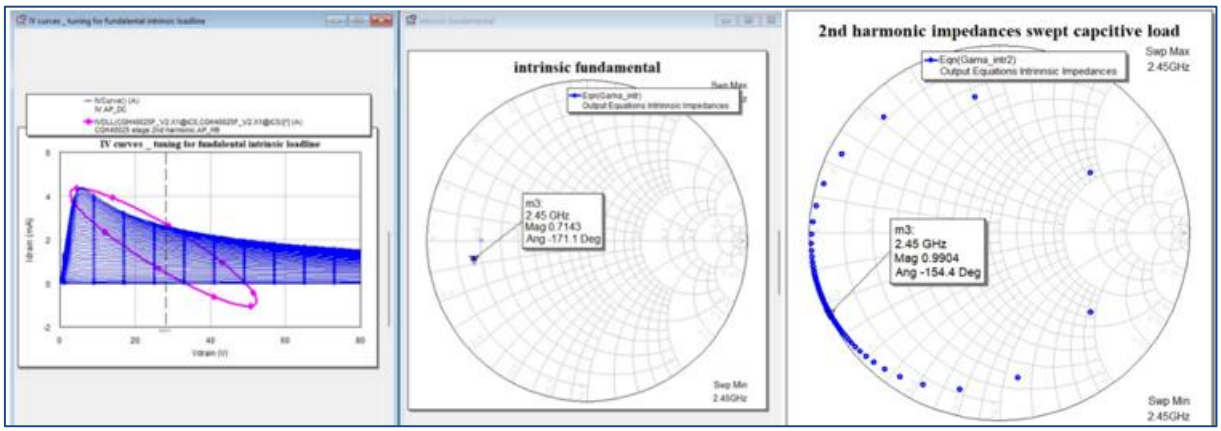


Figure 14

The important fact to observe here is that most of the 5-degree steps, because of the output transistor capacitor, have concentrated into about 20-degree very dense section with about 0.25- degree steps.

This effect is the essence on which this application note is based on.

If the intrinsic harmonic impedance is in this section the performance of the stage will be strongly insensitive to tolerances affecting the harmonic loads impedances. Even a very wide tolerance will not affect the overall performance. That, in modern speak is “anti-fragile”[1].

The bigger the transistor, the bigger the output transistor, and the stronger the effect. The compressed section becomes even smaller, as shown in the graph of Figure 15 where a 100W transistor is used.

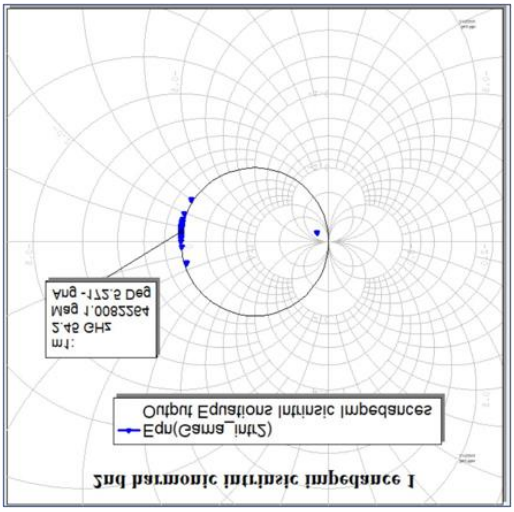


Figure 15

Conversely on the right of the Smith Charts of Figure 12, 13 and 14, a 5-degree step on the outside of the transistor leads to about 75-degree steps at the intrinsic generator. In Figure 15 it nearly doubles.

13. Move the harmonics intrinsic loads from being a short circuit (Class-B mode) to the middle of the dense section – Figure 16. Notice that the power and efficiency somewhat improve – Figure 17.

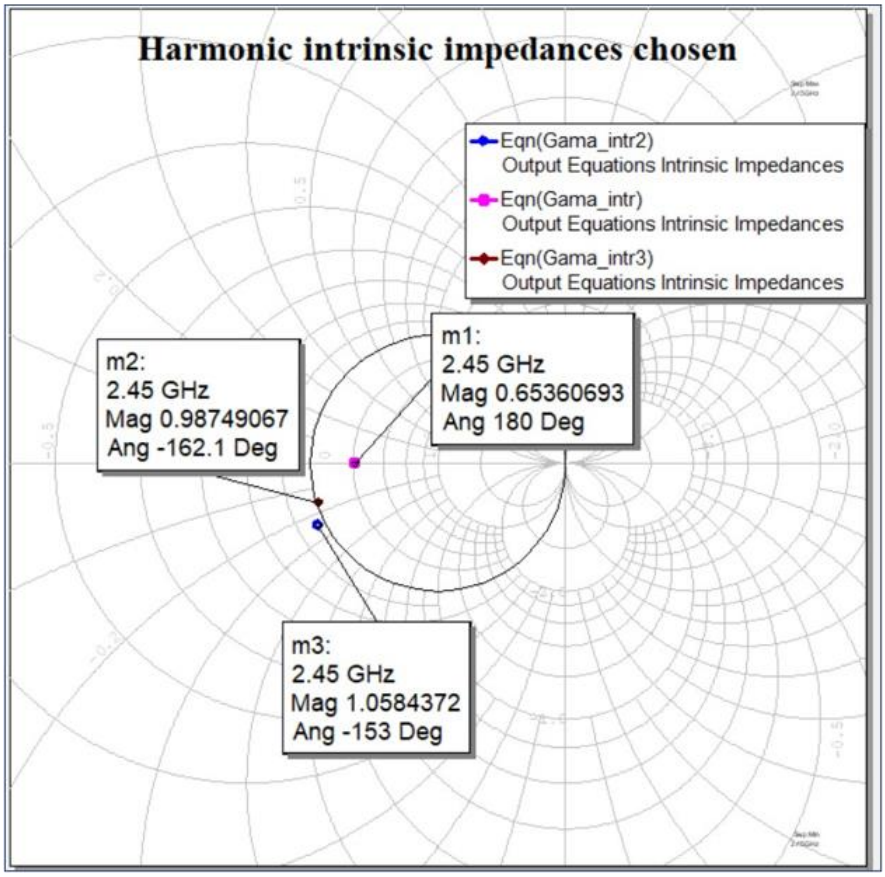


Figure 16

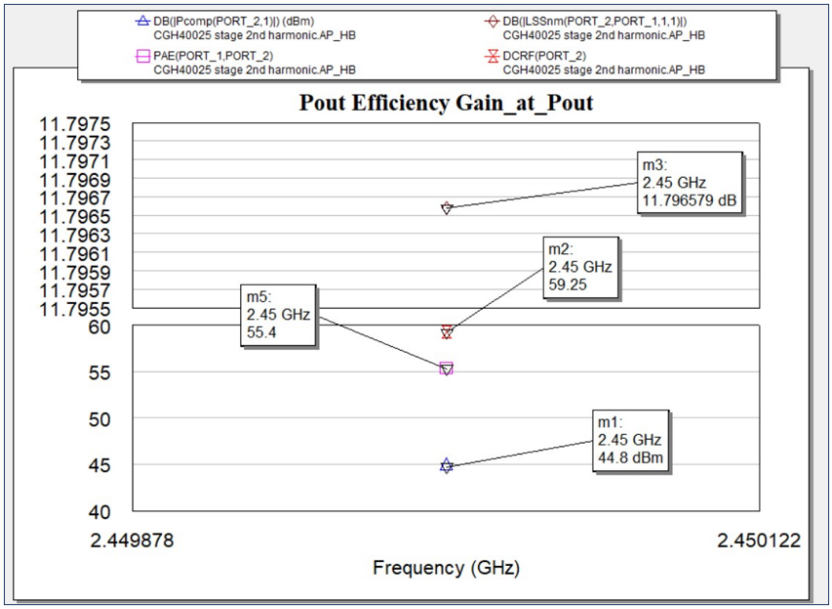


Figure 17

14. With the harmonics impedances selected in the middle of the dense sections tune the intrinsic fundamental impedance for maximum Pout. This greatly improves the efficiency also, as shown in Figure 18.

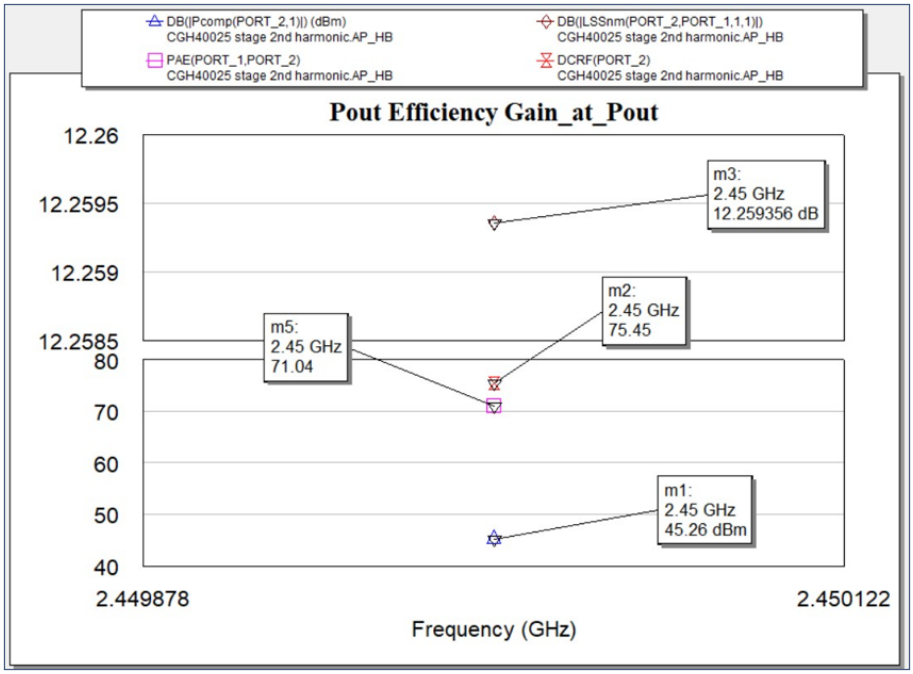


Figure 18

As a result of this last tuning on the Smith Chart can be seen that the corresponding intrinsic fundamental impedance becomes slightly inductive – Figure 19.

This happens to be the classic Class-J mode of operation, discovered, researched and explained by Steve Cripp in his book - [2]. Since at least 1983 Steve Cripps is teaching us how to understand and design RF power amplifiers properly.

Additionally the fundamental load could be tuned for maximum efficiency, which of course will be achieved at a different impedance than the one for maximum power.

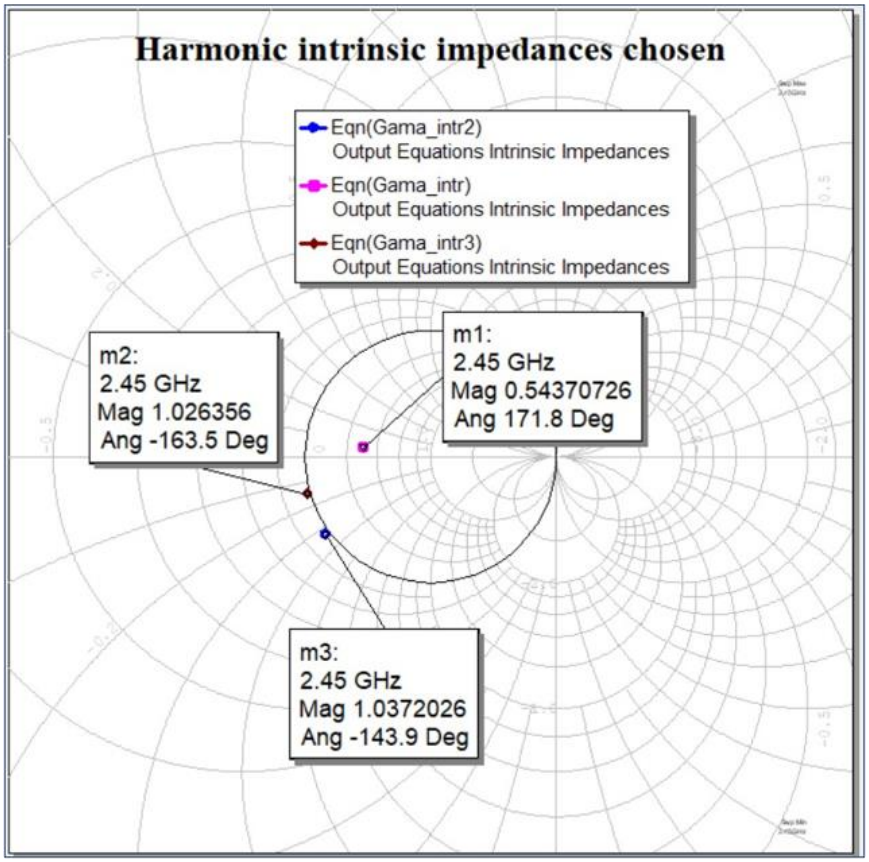


Figure 19

In theory, the same result could be achieved if the intrinsic 2nd and 3rd harmonic reactances are inductive and the fundamental intrinsic impedance is with capacitive reactance. This is going into the sensitive areas though, so leave this combinations to the PhD candidates and their professors.

15. With the inductive intrinsic fundamental load already achieved, sweep simultaneously the angles of the 2nd and 3rd harmonics load reflection coefficients fully 360 degrees with the 5 degrees steps – Figure 20.

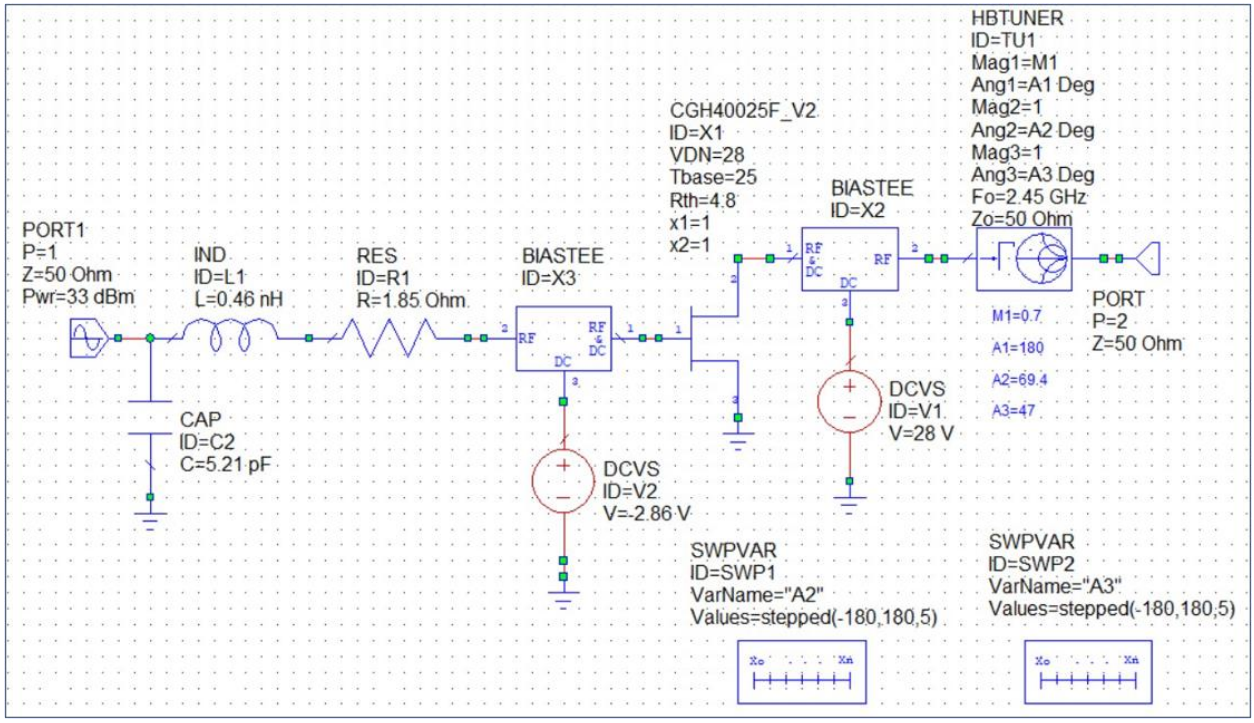
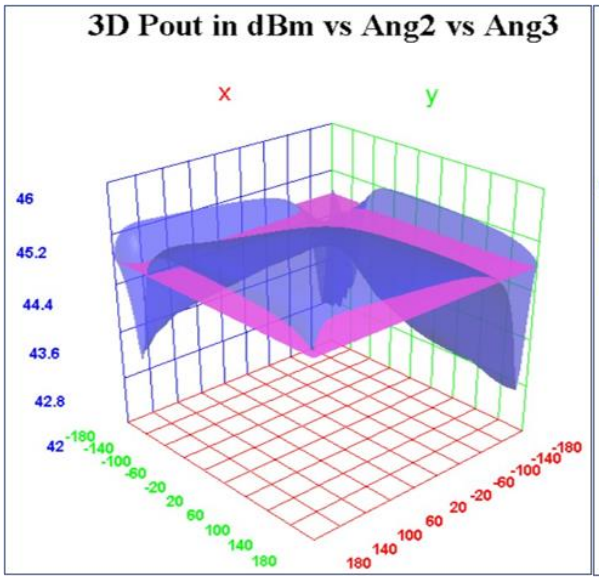


Figure 20

This simulation allows plotting of Pout and efficiency (drain efficiency in this case) on 3D graphs.

In the graphs of Figures 21 and 22 , the results of Pout and drain efficiency are displayed in blue, and reference plains of desired achievement in pink.



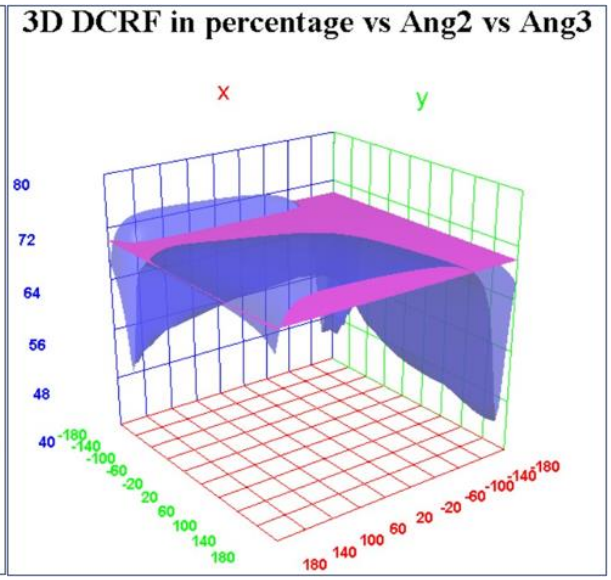


Figure 21 **Figure 22**

A schematic to simulate and plot the reference planes is in Figure 23. The difference for Pout and drain efficiency is only in the Pwr value of the input port.

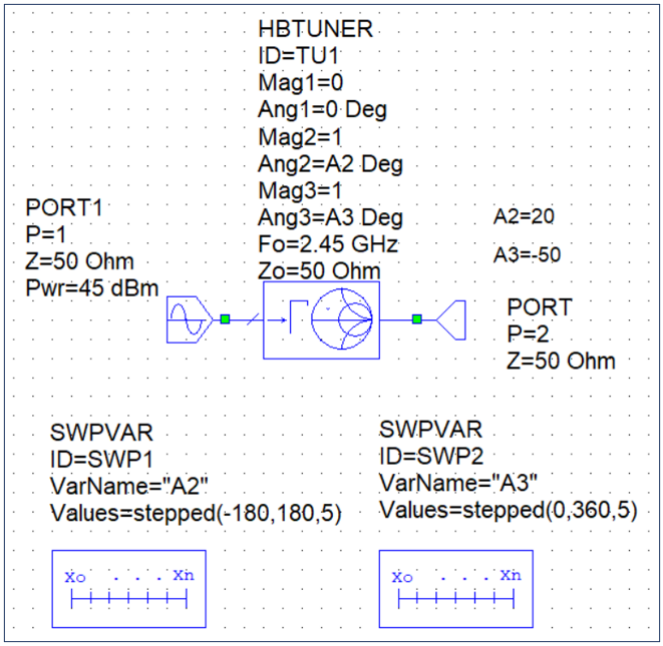


Figure 23

Note the sizable area of good performance for wide change of 2nd and 3rd harmonics reactance's (angles) of the load.

Most interesting is that these wide changes at the output terminal of the transistor define nearly same condensed areas at the intrinsic generator, shown on the Smith Charts in Figures 12 and 13, when the dips in the performance are in the stretched areas. This suggests that it is best to avoid the stretched areas where any small tolerance could cause trouble.

If one looks carefully it could be noticed that there is a narrow area where the combinations of fundamental and harmonics load impedance provides best performance for power or efficiency. But at least the 2nd harmonic load is again in the sensitive areas. And right next to this area are the dips in performance. It would prudent to avoid this “best” performance area too.

Procedure when the transistor model is a black box

This procedure follows naturally from the already discovered and presented above.

1. Again use only one ton in the optional properties of the harmonic balanced simulator.

2. Tune for maximum power to provide an intrinsic impedance to the intrinsic generator for Class-B. Although not possible to visualize it, it will be by necessity, by the law of nature, as was shown in Figure 7.

3. Switch back to 3 tones and simulate for the 3D graphs shown in Figure 21, 22 and 23.

4. Choose the 2nd and 3rd harmonic reactance values in the middle of the wide areas above the reference plains for required performance. This may not be as accurate as when seeing the reactance values at the intrinsic generator, but it is much better than not defining the 2nd and 3rd harmonic impedances.

5. Tune again the fundamental load impedance for maximum power or for maximum efficiency. It will be Class-J mode with inductive fundamental intrinsic load.

Design of the output matching network recommendations

Now, when the fundamental and harmonics loads are predefined for as many frequencies in an intended bandwidth, load-pull contours simulations could be properly performed as is described in reference [3] and shown in its Figure 7.

A versatile network synthesis tool should allow to synthesize for target areas of the fundamental and harmonic loads.

It might be also possible to directly used the defined here fundamental and harmonic loads without going for load-pull simulations.

In both cases the wider the required bandwidth the lower the weight factors should be for the 2nd and 3rd harmonic loads in the synthesis of the output network and the wider the area of the reactance allowed, but only in the congested non-sensitive areas as discussed here. The 3rd harmonic load has much less influence on the performance, so its weight factor should be lower than for the 2nd harmonic load.

The same is valid for the post synthesis optimizations.

The 3rd harmonic load could even be omitted for synthesis and optimizations. Especially if it is suspected that the parasitic elements of the transistor model at the 3rd harmonic frequency are not accurate. Typically, the package parasitic elements are represented with only a few lumped elements, but at much higher frequences this is distorting the reality. There are effects from the small transmission lines on the package which may not be modelled well with only a few lumped elements.

In any case it will be a good practice to see where the intrinsic loads are after the synthesized network is in place and during optimizations.

Conclusion

This application note introduces procedures for optimally defining the fundamental and the 2nd and 3rd harmonics load impedances for power or efficiency. Trying on purpose to place the harmonics intrinsic impedances in the condensed areas so that the output matching network at the harmonic frequences does not provide steep frequency slope or even resonates out the output the output capacitor provides an antifragile response to tolerances.

References

[1] Nassim Taleb, “Antifragile: Things That Gain from Disorder”, Random House, 2012

[2] Steve C. Cripps, “RF Power Amplifiers for Wireless Communications – Second Edition, Artech House, 2006

[3] Neal Tuffy et al., “A Simplified Broadband Design Methodology for Linearized High-Efficiency Continuous Class-F Power Amplifiers”, IEEE Transactions on Microwave Theory and Techniques, vol. 60, no. 6, June 2012

[4] Zulhazmi A. Mokhti et al., “The Nonlinear Drain–Source Capacitance Effect on Continuous-Mode Class-B/J Power Amplifiers”, IEEE Transactions on Microwave Theory and Techniques, vol. 67, no. 7, July 2019

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