cadence®

What's New in AWR Design Environment V22.1

Product Version 22.1

What's New in AWR Design Environment v22.1

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AWR Design Environment V22.1 What's New

What's New Organization

The Cadence® AWR Design Environment® V22.1 What's New document is organized into several sections:

- "*AWR Design Environment Features*" - Common improvements to all products.
- "*Microwave Office Features*" - Cadence Microwave Office design-specific software improvements.
- "*VSS (VSS) Features*" - Cadence Visual System Simulator™ (VSS) communications and radar systems design-specific software improvements.
- "*Migration Issues*" - Migration issues from previous versions to the current version.

Features listed in this document may also include links to videos or reference examples included in the AWR Design Environment platform installation. Examples are listed by file name, for example: *filename.emp*. To find an example in the AWR Design Environment platform, choose **File > Open Example** and type the example name.

Major Features Overview

Limited Release Features

The current release includes some "Limited Release" features. In an effort to get customer feedback on features we are developing, and to ensure that those features are successfully solving the full range of the intended real-world engineering problems, Cadence is releasing select features in this "Limited Release" state. These features, while in the software, may require a license to access. To use these features please contact your local Cadence Sales representative to obtain documentation and the appropriate license(s). Cadence strongly encourages you to provide feedback to ensure that these features work well and solve your engineering problems.

AWR Design Environment

- "Version Control Improvements": Bug fixes and improvements to the Design Sync and Cliosoft integration.
- "Schematic and System Editor Enhancements": New Swap Element dialog box and other improvements.
- "Python Scripting": Getting started with Python Scripting examples and articles.

Microwave Office

- "Silicon RF/mmWave IP Creation": Facilitate the design and analysis of RF/microwave, analog, and digital design elements together with Virtuoso platforms. This is a limited release feature.
- "EMX Planar 3D Solver Integration": Run EMX simulation of silicon RFIC designs from within the AWR Design Environment platform. This is a limited release feature.
- "Interoperability with Allegro Platforms Enhancements": Create and analyze RF/microwave IP in Microwave Office software and share schematic and layout with Allegro platforms. This is a limited release feature.
- "Enhanced SpectreRF Integration": Specify SpectreRF as the simulator for loadpull and VSS nonlinear model extraction. This is a limited release feature.
- "Optimizer Enhancements": New Pointer - Hybrid optimizer method and simplification of existing methods.
- "PCB Import Wizard": Improvements to the import of Allegro and Gerber format files.
- "Synthesis Wizards": The Component Synthesis Wizard and Mixer and Multiplier Synthesis Wizard are now unlicensed.

- "Clarity 3D Solver Integration": Integration of the Cadence Clarity™ 3D Solver enables direct simulation of 3D EM structures from within the AWR Design Environment platform.
- "Celsius Thermal Solver Integration": Run thermal analysis directly on structures created in the AWR Design Environment platform.
- "Nimbix Cloud Support": Run Cadence AXIEM® 3D planar EM solver and Cadence Analyst™ 3D FEM EM solver in the cloud.
- "Mixer Design": Application content for mixer designers.
- "RF Measurements": RF measurement related application content.

VSS

- "Data File Improvements": Smoother flow of co-simulating between VSS software and other external tools.
- "Amplifier Design": Application content for amplifier designers
- "Mixer Design": Application content for mixer designers.
- "RF System Design": Application content for RF system designers.
- "RF Measurements": RF measurement related application content.

AWR Design Environment V22.1 Licensing and Operating System Changes

See "Licensing Changes" for licensing and OS migration details.

AWR Design Environment Features

The Cadence® AWR Design Environment® V22.1 software includes the following new features, enhancements, and user interface changes. These changes are common to the Cadence Microwave Office® software and Cadence Visual System Simulator™ (VSS) communications and radar systems design software.

Version Control Improvements

The AWR Design Environment platform supports integration of version control software to effectively manage group design of complex, multi-function projects on many different technologies. You can use version control to easily collaborate between multiple designers and keep revision history of design data. Improvements in this release include:

- Additional support for Layer Process File (LPF) and custom symbol file types.
- Enhanced document import error-handling, specifically targeted to missing or incorrectly versioned PDK's.
- Ability to revert to a specific revision using the History dialog box.
- Design Sync integration support for file-based vaults and module-based vaults.
- Cliosoft integration revision now shows **Rev ID** instead of **Revision**, and status is now correct.
- The **Use project defaults** option is now unchecked for items added to version control to ensure identical behavior between projects.
- Disabled subcircuits are now included in the hierarchy check.
- Pressing **Escape** now closes the Version Control dialog.
- Global Definitions documents now retain their version-controlled status when moved in the Project Browser.
- Repositories no longer disappear from the Version Control dialog box if an LPF for an EM structure is added to source control.

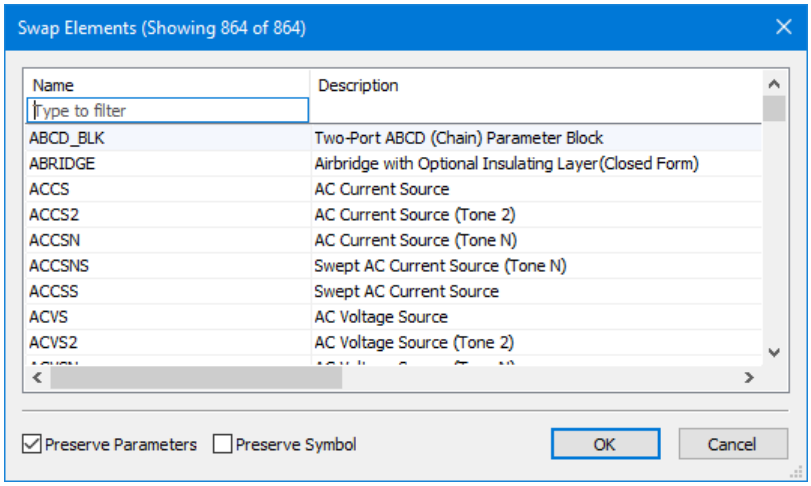
Additional Information:

- Documentation: "Using Version Control".

Schematic and System Editor Enhancements

Improvements to the Schematic and System editors:

- Upgraded the Swap Elements dialog box with filtering capabilities and check boxes that enable preservation of parameters and/or symbols.

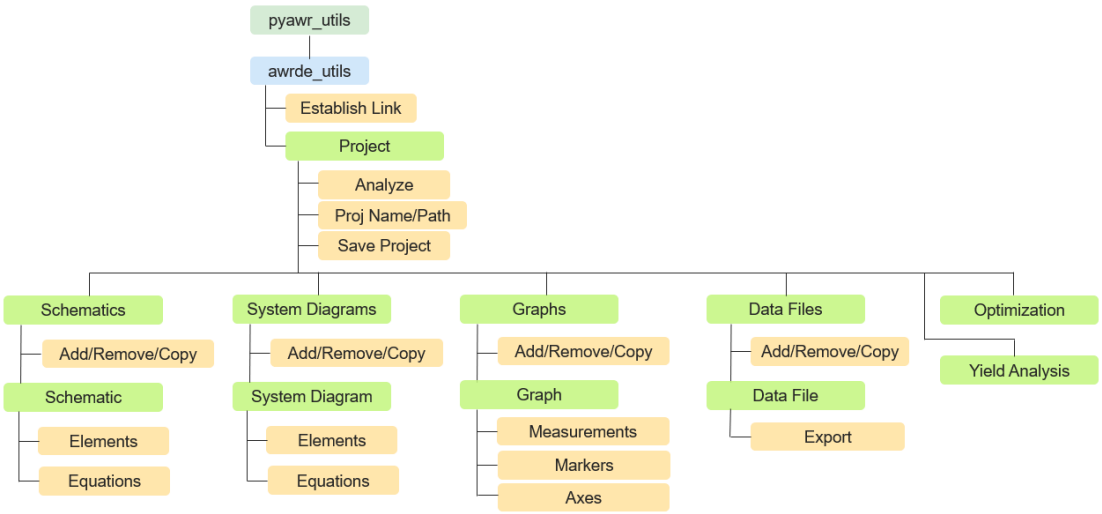


- Added a **View > Major Grid Markers** command (schematic editor only).

Python Scripting

Added material to assist users with Python scripting:

- AWR Knowledge Base: Python Landing Page. Includes a complete listing of Python related content in the AWR Knowledge Base.
- Article: Pyawr Utilities. Getting Started guides for using Python as a scripting language for the AWR Design Environment software.



- Python Script: Pyawr Utilities Examples. Example code using pyawr-utilities.
- Python Script: Python Scripting with AWR Design Environment: 2D and 3D Plotting with Swept Variables. Use a Python module to extend graphing and visualization capabilities outside of AWR Design Environment capabilities. software.

Microwave Office Features

Cadence® Microwave Office® software V22.1 includes the following new features, enhancements, and user interface changes. The Cadence AWR Design Environment® platform changes also apply to these specific products.

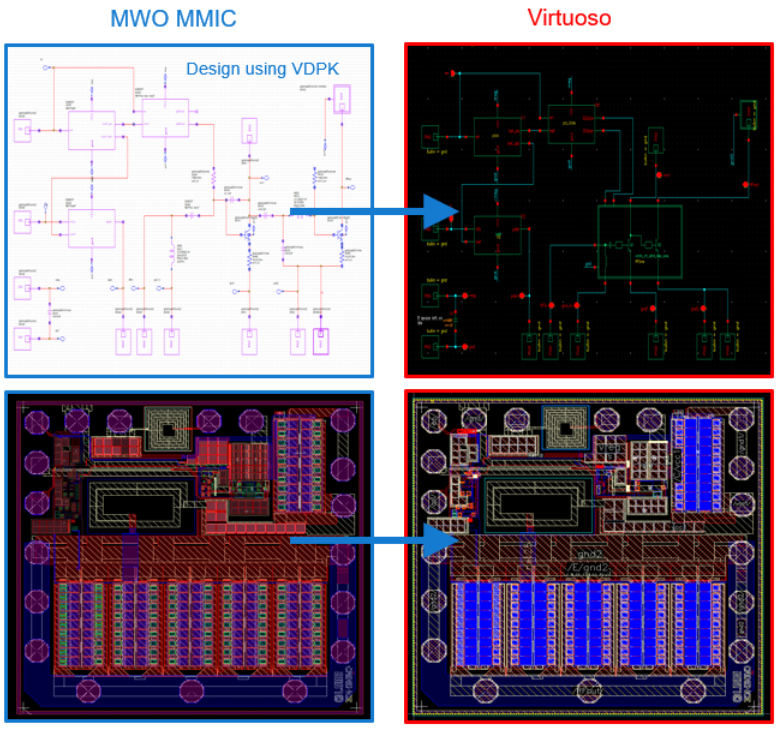
Silicon RF/mmWave IP Creation

The AWR Design Environment platform now offers an RF/microwave design creation environment with an export pathway to Cadence Virtuoso® Schematic Editor and Cadence Virtuoso® Layout Suite. You can now create and analyze Silicon RF/mmWave IP utilizing Virtuoso PDKs in Microwave Office software, and share the schematic and layout with Virtuoso software ready for analysis, design integration and backend verification flows. Interoperability between these software tools facilitates the design and analysis of RF/microwave, analog, and digital design elements together.

NOTE: This is a limited release feature.

Improvements to Virtuoso interoperability in this release include:

- Support for Virtuoso PDK reuse in Microwave Office software, which now reads and executes the same SKILL based PDK as Virtuoso software.
- Designs created in Microwave Office software with Virtuoso PDKs utilize the MWO Unified database.
- Support for remote EMX simulation of Virtuoso PDKs on Linux.
- Improved export validation checking (choose **Scripts > Unified Library**).



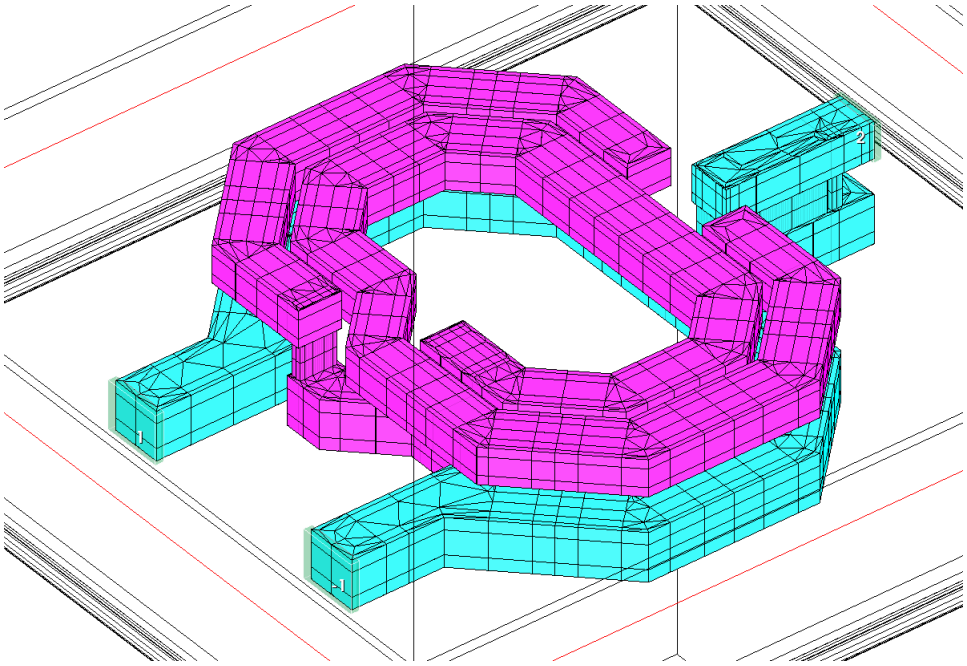
Additional Information:

- Documentation: "AWR Design Environment/Virtuoso Interoperability ".

EMX Planar 3D Solver Integration

Run electromagnetic analysis on silicon Virtuoso PDK RF circuit designs from within the AWR platform using the Cadence EMX® Planar 3D Solver. The EMX solver is extremely efficient and accurate at solving silicon IC structures and is widely supported by foundries.

NOTE: This is a limited release feature.



Additional Information:

- Documentation: "EMX Planar 3D Solver".

Interoperability with Allegro Platforms Enhancements

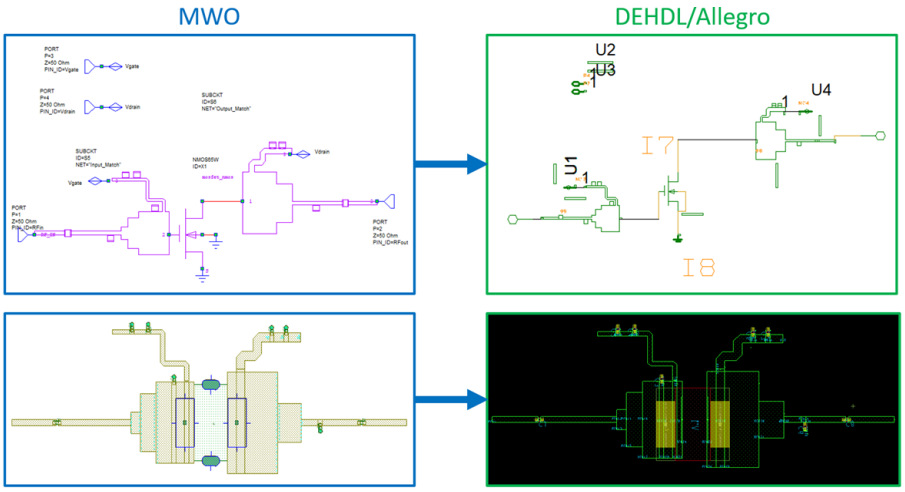
The AWR Design Environment platform supports a broader PCB subsystem design flow with an integrated flow between Microwave Office software and Cadence Allegro® PCB design tools. You can now create and analyze RF/microwave IP in Microwave Office software, with the schematic and layout shared with Allegro/DE-HDL software. Interoperability between these software tools facilitates the design and accurate and fast simulation of complex PCB subsystems.

NOTE: This is a limited release feature.

Improvements to Allegro interoperability in this release include:

- Support for the Allegro Reference Library format. The support for previous Combined Library format is now deprecated.
- User-friendly cell names in XML.
- A new MVIA2P element to support interoperability.
- DE-HDL/Syscap symbol pin names now display in Microwave Office software.

- Improved export validation checking (choose **Scripts > Unified Library**).

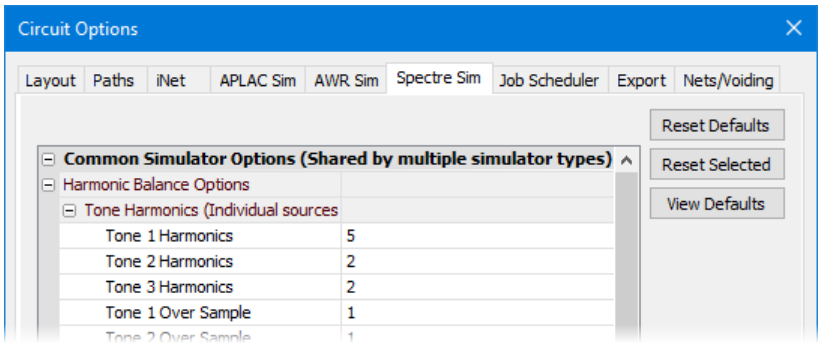


Additional Information:

- Documentation: "AWR Design Environment/Allegro Interoperability ".

Enhanced SpectreRF Integration

It is now easier to set up SpectreRF simulation in the AWR Design Environment platform with a new Circuit Options dialog box**Spectre** tab.



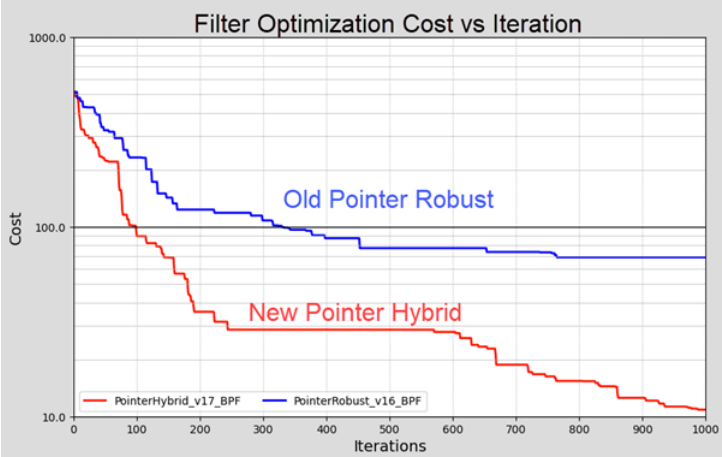
Additional SpectreRF harmonic balance improvements include:

- Support for SpectreRF as a loadpull simulator.
- Support for SpectreRF as a simulator for NL_S and MIXER_S blocks for VSS nonlinear model extraction.

NOTE: This is a limited release feature.

Optimizer Enhancements

A new Pointer - Hybrid optimizer method is introduced which combines the best performance of several optimizers to produce a top-performing algorithm on a very wide range of problems.



Additional optimizer method improvements include:

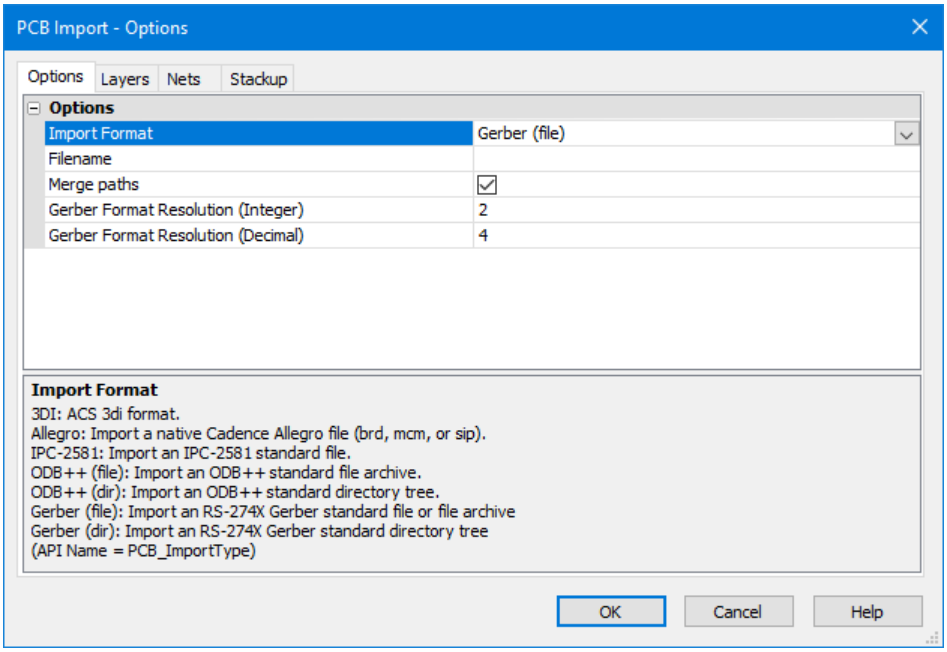
- The Grid Search (previously Discrete Local) method now works with continuous variables using a new **Auto # Steps** parameter that automatically discretizes variables.
- The Differential Evolution method now has self-adapting parameters, making it easier to use. It also now works with discrete variables
- All methods except for Lineup and Gradient can now run in parallel.
- All methods except for Lineup and Gradient can now use the **Step Size** parameter defined on variables.
- The optimizers are now ordered in the selection list in order of recommendation.
- Parallel and single-thread versions of optimizers are combined.
- Optimizer names are revised for clarity.

Additional Information:

- Documentation: "Optimization Methods".
- Map of V16 optimizers to V22.1 equivalents: "Optimizer Methods"

PCB Import Wizard

The PCB Import Wizard enables import of 3Di, Allegro, IPC-2581, ODB++, and Gerber (X1 and X2) standard files into the AWR Design Environment software platform.



Improvements to the PCB Import Wizard in this release include:

- Gerber import now supplies a default aperture if none is specified in the file.
- Gerber import now correctly handles arcs specified with relative endpoints.
- Allegro software *.brd* import has improved error reporting.

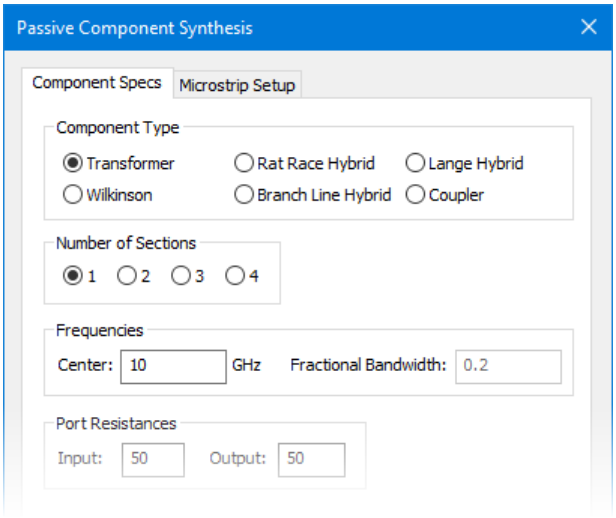
Additional Information:

- Documentation: "PCB Import Wizard".

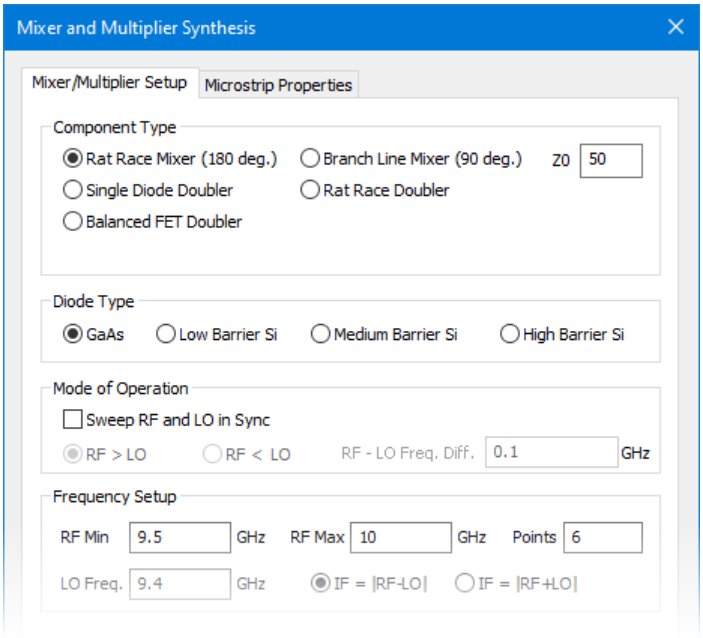
Synthesis Wizards

The Component Synthesis Wizard and the Mixer and Multiplier Synthesis Wizard no longer require additional licensing and are now available to all users.

The Component Synthesis Wizard allows you to synthesize several types of passive microwave structures to be implemented in microstrip transmission line structures.



The Mixer and Multiplier Synthesis Wizard allows you to synthesize several types of mixer and multiplier structures to be implemented in microstrip transmission line structures.



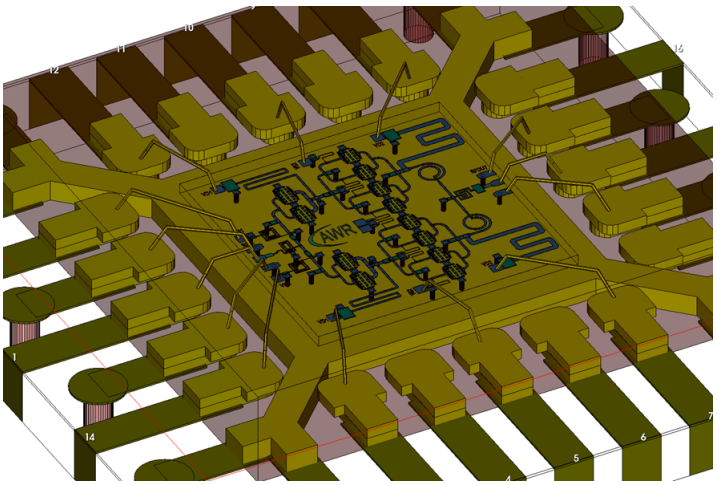
Additional Information:

- Documentation: "Component Synthesis Wizard".
- Documentation: "Mixer and Multiplier Synthesis Wizard".

Clarity 3D Solver Integration

Simulate EM structures from within the AWR Design Environment platform using the Cadence Clarity™ 3D Solver, a 3D full-wave electromagnetic (EM) simulation software tool. Clarity has the ability to solve much larger problems such

as entire modules and complete BAW/SAW filters with greater speed. Clarity integration now supports simulation on clusters.

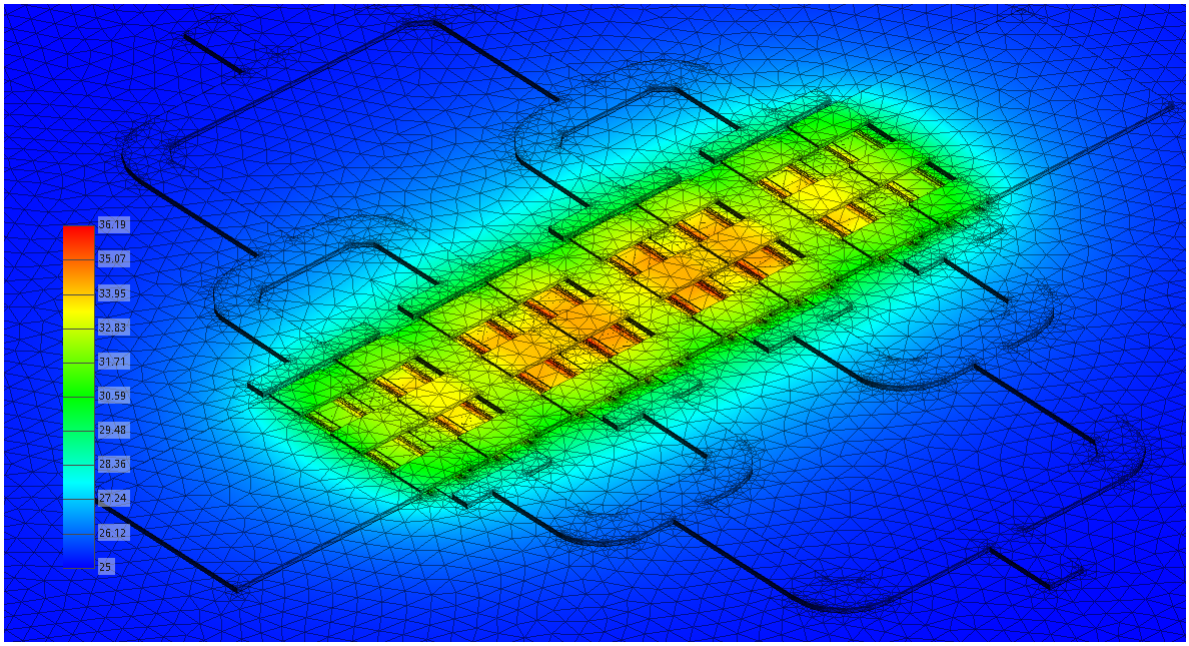


Additional Information:

- Documentation: "Clarity 3D Solver".

Celsius Thermal Solver Integration

Run thermal analysis from within the AWR Design Environment platform using the Cadence Celsius™ Thermal Solver. You can create Celsius EM structures by either drawing the geometry in the EM editor, or by using EM extraction. After simulating, open the structure in the Celsius native editor to view 3D field plots of the thermal temperature distribution. Temperature results of the Celsius simulation are returned to the AWR Design Environment platform.

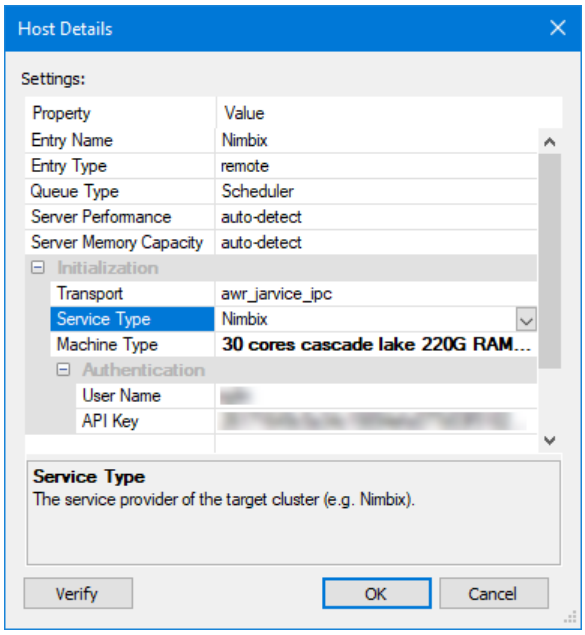


Additional Information:

- Documentation: "Celsius Thermal Solver".

Nimbix Cloud Support

Remote Cadence® AXIEM® 3D planar EM solver and the Cadence Analyst™ 3D FEM EM simulations on the Nimbix Cloud is now supported.



NOTE: This is a limited release feature.

Mixer Design

Application content for mixer designers includes:

- Article: Mixer Noise in MWO and VSS. How to set up a harmonic balance simulation for mixer noise analysis and how to build a mixer subcircuit out of base components that generates LO harmonic mixer noise.

RF Measurements

RF measurement-related application content includes:

- Python Script: TDR Gating Python Script. Replicate the VNA instrument TDR gating functionality to mathematically remove discontinuities from measured S-parameter data.
- Python Script: Using the Negation Element in AWR and Python to Speed Up Device Characterization. How to efficiently characterize a reconfigurable network without simulating every configuration.

Minor Improvements

Microwave Office V22.1 software includes the following minor new features, enhancements, and user interface changes.

New Circuit Models

The following new circuit models are included in Microwave Office v16 software.

Microstrip Components

- "Cylindrical Two Port Via with Microstrip Pad (Closed Form): MVIA2P "

API

- Added Exists2 and Item2 methods off of the CProcessLibraries collection. These methods both take library name and library version string parameters, so that a specific version can be selected.
- Added API access to the EM Port Material property and EMPort InfoText which provides access to the information on the **Info** tab of the EM Ports Properties dialog box.
- Added direct access from an EMStructure to the DesignRuleChecker object (EMStructure.DesignRuleChecker).
- SystemDiagrams.Import() no longer links to a system diagram rather than embedding it.
- An API error is now issued instead of crashing when attempting to use the linked file Save method with an embedded document.
- Add a new element.copy method that copies elements in a schematic or a Global Definitions document.
- Updated the DataFile export method to accept a folder as the target location for export.

Cell Libraries

- Cell libraries which link to a file in a PDK are now always updated to point to the currently loaded version of the PDK, even after changes to the PDK version in a project.

Equations

- Equation function DataFileCol() can now access columns of string values in DSCR files.
- Undo of an equation deletion now restores the Parameter Definition settings of the equation.

Graphs

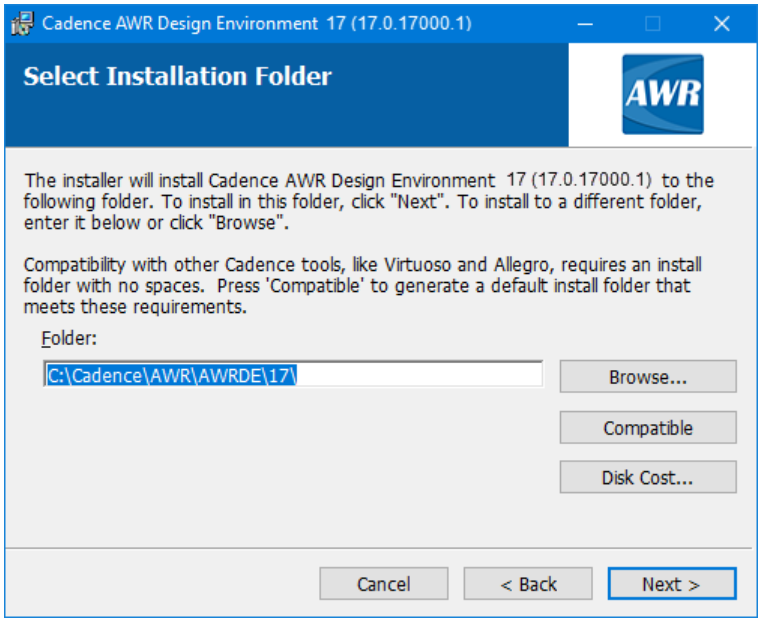
- Offset marker are now consistently placed on the correct side of the reference marker if the offset is small.

Global Definitions

- Fixed problems with parameter value scaling and the LPF setting on global definitions documents when the documents are imported into a project.
- The options for global definitions documents are now read-only if the document is read-only.
- Moving a linked global definitions document in the Project Browser hierarchy now functions properly.

Installation/Licensing

- You can now select a Cadence compatible installation location by clicking **Compatible** in the Select Installation Folder dialog.



Job Scheduler

- Improved the reconnection reliability between a user computer and scheduler node after a user computer awakens from sleep or hibernation.

Layout

- Added a **Hide/Show Upper Level Flightlines** command to the Edit-in-place operation context (right-click) menu.
- Upper level flightlines now draw dimmed when descending in hierarchy using edit-in-place operations.
- Added new FrozenMarker and AnchorMarker system layers, which allow flightlines on the RatsNest to be turned off while frozen, and allow anchor markers to remain visible.
- Users are now prevented from replacing the default LPF in a project with an EM LPF, which could result in crashes.
- Cutlines no longer cause false DRC errors.

Layout - EM

- The STACKUP now correctly displays units of the LPF it is referencing rather than the units of the LPF referenced by the Global Definitions or schematic document in which it is placed.
- 3D EM parts are no longer scaled incorrectly when the parent EM structure is not using the same units as the default LPF.
- The size of a custom wave port generated through EM extraction now matches the custom wave port size set on the corresponding extraction port in schematic layout.
- When exporting a schematic layout as a GDSII file, flat or hierarchical, any Analyst EM structures contained as subcircuits are now also exported. Note that arbitrary 3D EM structures are not exported. This enhancement is generally intended when Analyst structures are used as SUBCKTs in a circuit schematic with common drawing layers and EM layer mapping. Any new drawing layers created in the Analyst SUBCKTs are also automatically added to the schematic lpf and GDSII file export mapping and thereby are exported by default with the main schematic.

- The Add Element dialog box (**Ctrl+L**) can now be used to place XML-defined elements in EM schematics.

Libraries

- Added component library XML support for Generalized MDIF data files.

Load Pull

- The Version list in the Select Process Library dialog box now updates immediately after users browse for a library.
- Updated the Load Pull script to use LPF units rather than project units.

Measurements

- Fixed an error with measurements on an MDIF data file when FPRJ did not match FDOC. Also improved the error message when there are not enough samples for parameter interpolation.

Models

- Fixed DBU (layout) rounding errors with the GM1LIN element.

Netlists

- PSpice netlist import now supports "+" and "-" as node names.

Schematic Editor

- When pushing into a SUBCKT using the **Edit Subcircuit** command, you can now choose which Switch View document to push into when available.

Simulation - Nonlinear

- The **Simulate > Results** command and Save Simulation Results dialog box are no longer available. Simulation results are available as simulation data sets in the Project Browser **Data Sets** node.

Simulation - APLAC

- Added a new APLAC Stability option, **Gamma probe level**, to control the calculation method used for gamma probes.

Simulation - Clarity

- The **Min Iterations** setting no longer falls below the minimum threshold when converting an Analyst structure to Clarity.
- The Clarity integration now supports dashes in the project name.

Tuning, Yield Analysis and Optimization

- The full path and project name is now included in the **Setup** section of the optimizer log file.
- The limit on the number of variables allowed for User Defined corners analysis has been removed.

User Interface

- The **Find Next** button in the **Find** function on the Variable Browser **All** tab now functions correctly when there are multiple search text matches in the same cell.

Wizard - PCB Import

- Fixed an ODB++ import issue that caused missing pin designations.

VSS (VSS) Features

The Cadence® Visual System Simulator™ (VSS) communications and radar systems design V22.1 software includes the following new features, enhancements, and user interface changes. The Cadence AWR Design Environment® platform changes also apply to this product.

Data File Improvements

This release introduces new data file utilities to simplify exporting and importing of waveform data for applications such as DPD, DUT evaluation, and communications receiver testing. The updated FILE_SNK block can capture multiple waveforms, which can be used in HW or external applications. In return, waveforms captured from HW or other applications can be imported into VSS using the new FILE_SRC block. To facilitate signal demodulation in VSS, transmitter-generated signal properties are used; the new PPROP_SAVE and PPROP_LOAD blocks can save and re-apply propagated properties from and to any signal in VSS, and are designed to work in conjunction with FILE_SNK and FILE_SRC. These new capabilities provide a much smoother flow of co-simulating between VSS and other external tools.

Additional Information:

- Documentation: "File Capture: FILE_SNK".
- Documentation: "File Source: FILE_SRC".
- Documentation: "Propagated Properties Save: PPROP_SAVE".
- Documentation: "Propagated Properties Load: PPROP_LOAD".
- Example: *Data_File_Capture_and_Replay.emp*

Amplifier Design

Application content for amplifier designers:

- Python Script: VSS AMP_F File Creation. Easily create both frequency-dependent and power-dependent text files from a manufacturer's data sheet for use with the VSS AMP_F element.
- Article: VSS Noise in a Power Combined Amplifier. Explanation of noise offset in power combined amplifiers and mitigation techniques to reduce the offset.
- Article: Power Combination. Tutorial on the difference between coherent and non-coherent signal combination in power amplifiers and an explanation of vector addition of multiple non-coherent signals.

Mixer Design

Application content for mixer designers:

- Article: Mixer Noise in MWO and VSS. How to set up a harmonic balance simulation for mixer noise analysis and how to build a mixer subcircuit out of base components that generates LO harmonic mixer noise.
- Python Script: VSS RFI Heritage XML File Parser. Parse the RF Inspector Heritage window data and save it to an Excel spreadsheet for more efficient analysis.
- Article: VSS IQ Mixer Model. How to model data sheet-specified IQ upconverter and IQ downconverter mixers using base VSS elements.

RF System Design

Application content for RF system designers:

- Article: VSS Phase Noise Simulations. How to configure system diagram settings and phase noise measurement parameters to speed up simulation time without sacrificing accuracy.
- Article: Cascade Analysis: Optimizing RF Systems for Dynamic Range. Tutorial on RF chain cascade analysis (noise figure, IP3, P1 dBm as a signal progress through an RF system) and strategies for optimizing a chain for noise figure and IP3.
- Article: VSS C_HDRM (Cascaded Headroom) Measurements. Learn how to use the VSS RF Budget analysis Cascaded Headroom (C_HDRM) measurement.
- Python Script: VSS RFI Heritage XML File Parser. Parse the RF Inspector Heritage window data and save it to an Excel spreadsheet for more efficient analysis.
- Article: VSS Power Spectrum Measurements: FFT Windowing Effects. Tutorial on the effects of windowing in VSS spectrum measurements to assist in choosing the best windowing type for a particular system.
- Article: Power Combination. Tutorial on the difference between coherent and non-coherent signal combination in power amplifiers and an explanation of vector addition of multiple non-coherent signals.

RF Measurements

RF measurement related application content:

- Article: VSS Phase Noise Simulations. How to configure system diagram settings and phase noise measurement parameters to speed up simulation time without sacrificing accuracy.

Minor Improvements

VSS V22.1 software includes the following minor new features, enhancements, and user interface changes:

New/Updated System Blocks

The following new system blocks are included in VSS V16 software.

Data File Blocks

- "File Source: FILE_SRC"
- "Propagated Properties Save: PPROP_SAVE"
- "Propagated Properties Load: PPROP_LOAD"

Data Files

- SMPSYM is now recognized as a data file header similar to SMPFRQ, TSTEP, CTRFRQ, and others.

Measurements

- The alignment of the block symbols displayed in RF Budget Analysis graphs is improved, particularly when a block is flipped or reversed.

System Block Updates

- When AMP_F is configured to generate DCPOUT and the data file/IMPLTYP settings result in an AM/AM-AM/PM model being used, the DCPOUT value is no longer always 0 for RF Budget Analysis and RF Inspector simulations.
- When PORT_SRC sweep is set to "Vector" while the vector defining PWR consists of a single value, simulation results now update correctly with changes to the PWR value.
- When using the default symbol generated by the LIN_S block, if the LIN_S block has three or more ports assigned and the port assignments are changed but the number of ports assigned as input ports and as output ports do not change, the symbol now updates to show the new port assignments. Note that the name of the default symbol generated by the LIN_S block now includes the port assignments, previously it did not.
- When the LIN_S block has multiple output ports configured it now uses the S matrix of the block at the current center frequency to determine the path cost used to select the signal path for RF Budget Analysis simulations. If frequency sweeping is desired, a SWPVAR block should be used instead of sweeping frequencies via the document or project frequencies from the **RF Frequencies** tab, as sweeping via the document or project frequencies does not in fact sweep the center frequencies.

System Diagrams

- Project Import now switches to using the local **Dependent parameters use base units** document option for imported system diagrams.

Wizards - Amplifier Model Generator

- Corrected the Amplifier Model Generator Wizard EVM calculation in the case of many IQ and AM-AM/PM files or data blocks.

Wizards - Phased Array Generator

- The schematic layout generated from Phased Array Generator now has the correct steering angle sign, which now matches the generated system diagram and data file.

Migration Issues

The following are issues you need to address when migrating from a Cadence® AWR Design Environment® platform V16 release to an AWR Design Environment platform V22.1 release. Not all topics apply to every user. If you are not familiar with a topic or program feature included here, it probably does not apply to your use of the software. You should read about all of the issues before developing your migration strategy. The path to the <Appdatauser> files referenced in this document is operating system dependent. To view the directory path to your <Appdatauser> files, choose **Help > Show Files/Directories** to display the Directories dialog box, then double-click the *Appdatauser* folder.

AWR Design Environment V22.1 Specific Migration Issues

Licensing Changes

- The Component Synthesis Wizard and Mixer and Multiplier Synthesis Wizard no longer require a separate feature in the license file and are now available to all users. A nonlinear simulation license feature is required for the Mixer and Multiplier Synthesis Wizard, however, in order to run the nonlinear circuit simulations.

Optimizer Methods

In AWR Design Environment platform V22.1 software, the optimizer list is reorganized and reduced to simplify selection. The following optimizer table maps V16 software optimizers by name to their equivalent in V22.1 software.

V16 Optimizer	V22.1 Optimizer Equivalent
Advanced Genetic Algorithm	Adv Genetic Algorithm
Conjugate Gradient	Gradient Optimization
Differential Evolution	Diff Evolution
Direction Set Method	Gradient Optimization
Discrete Local Search	Grid Search
Genetic (Gaussian Mutation)	Adv Genetic Algorithm
Genetic (Uniform Mutation)	Adv Genetic Algorithm
Gradient Optimization	Gradient Optimization
Kapu Optimizer	Kapu
Lineup Optimizer	Lineup Optimizer
Parallel Advanced Genetic Algorithm	Adv Genetic Algorithm
Parallel Kapu	Kapu
Parallel Particle Swarm	Particle Swarm
Parallel Random Local	Random
Parallel Robust Simplex	Robust Simplex
Particle Swarm	Particle Swarm
Pointer - Gradient Optimization	Pointer - Hybrid
Pointer - Robust Optimization	Pointer - Hybrid
Random (Global)	Random
Random (Local)	Random

V16 Optimizer	V22.1 Optimizer Equivalent
Robust Simplex	Robust Simplex
Simplex Optimizer	Robust Simplex
Simplex Optimizer (Local)	Robust Simplex
Simulated Annealing (Simplex)	Robust Simplex

Note that all optimizers except Lineup and Gradient:

- Can run in parallel
- Can use discrete variables and step-sizes
- Now require variable constraints

The new optimizers are tested and found to perform as good as or better than the older optimizers they are mapped to, with no loss of capability on a wide range of problems. Note, however, that there may be exceptions. If an optimizer that is no longer available is required to achieve the best performance on a particular problem, contact Cadence Technical Support for assistance.

Unconstrained variables defined in older projects must be updated with constraints in order to work with the new optimizers. The following are steps to quickly add constraints:

1. Open the Variable Browser (choose **View > Variable Browser**).
2. Type "`1`" in the **Optimize** column header to filter on optimized variables.
3. **Shift**-select all the displayed variables.
4. Select the **Constrained** check box for the last selected variable to update the check box for all the selected variables.
5. Enter lower and upper bounds for the variables as a percentage or absolute delta of the current value by following the lower and upper bound value with a "%" or "#" sign respectively. For example, to enter a lower bound that is 10 percent lower than the current value for all the variables, type "`10%`" in the **Lower** column for the last selected variable.

Simulation - Nonlinear

- The **Simulate > Results** command and Save Simulation Results dialog box are no longer available. Simulation results are available as simulation data sets in the Project Browser **Data Sets** node.

Version-Independent Migration Issues

The items in this section address moving files and settings from one software version to another. Some of these files and settings are automatically migrated. If the previous software version is not found, up to three major versions back are searched. For example, if migrating to the AWR Design Environment platform V22.0, AWR Design Environment platform V16, AWR Design Environment platform V15, and AWR Design Environment platform V14 software are searched.

NOTE: Ensure that your Windows® Explorer program is set to show hidden and system files.

Files Automatically Migrated

The *Appdatauser* and *Appdatacommon* folders must be in their default locations for files or directories to auto-migrate. Changing their default locations would necessitate creating a *redirect.ini* file in the program directory, and is not a common practice.

Files in Appdatacommon

The migration of Appdatacommon is triggered based on the existence of the *mwoffice.ini* file in the *Appdatacommon* folder for the newly installed version.

- If there is an existing *mwoffice.ini* file, no files or folders are migrated.
- If the *mwoffice.ini* file does not exist, it is copied from the previous location if found.
- If the *mwoffice.ini* file does not exist and an older version is not found, a new file is created.

The path to each PDK is stored in the *mwoffice.ini* file and is available for any user of that computer. The installation location of foundry libraries is typically version-independent; the default installation locations are not dependent on the AWR Design Environment software version. These paths are used when opening a project using a PDK or by choosing **File > New with Library**.

All additional files and directories at this location are not copied since they should not be used with the new version of the software.

Files in Appdatauser

The migration of Appdatauser is triggered based on the existence of the *user.ini* file in the *Appdatauser* folder for the newly installed version. If there is an existing *user.ini* file, no files/folder are migrated. No existing files or folders are overwritten.

The following files/folders are migrated:

- All *.ini* files located at the top level directory of *Appdatauser*, including *user.ini*. The *user.ini* file contains environment settings, custom layout modes, and other environment defaults.
- All XML files located at the top level directory of *Appdatauser*. This includes:
  - *customizations.xml* - contains your hotkey settings.
  - *UICustomizations.xml* - contains your menu settings. You can reset the menus to the AWR Design Environment platform V15 defaults.
  - *UIDockingLayout.xml* - contains settings for how different windows are docked in the AWR Design Environment platform.
  - *UIToolBarLayout.xml* - contains your toolbar settings. You can reset the toolbars to the AWR Design Environment platform V15; defaults.
  - *materialdefs.xml* - There are several pre-set materials such as FR4, alumina, and GaAs available in the EM interface. If you modify these settings, the changes are stored in *materialdefs.xml*.
- These directories:
  - *scripts* - Global (available in any project) Visual Basic scripts.
  - *models/model64* - Custom models used in the AWR Design Environment platform.
  - *cells/cells64* - Custom cells used in the AWR Design Environment platform.
  - *symbols* - Custom symbol files created in the AWR Design Environment platform.
  - *em_models* - User-filled X-model tables.
  - *XML* - XML libraries installed in the default location.

All additional files and directories in this location are not copied since they should not be used with the new version of the software.

Files NOT Automatically Migrated

User-Defined XML Libraries

TARGET: Users who have local XML libraries (anything outside of the AWR web library)

- Many users either choose to install a local copy of the XML libraries or add to the default installation with other vendor-specific XML libraries. The default location is the <*Appdatauser*> folder. If your XML is in this location it can be migrated automatically (see "Files Automatically Migrated ").
- Starting in AWR Design Environment platform V11, the correct location for these libraries is *:\Users\UserName\AppData\Local\AWR\Design Environment\V11.0\XML*. There are top level folders for *3D EM Elements*, *Circuit Elements* and *System Blocks*. Any XML file located in these top level directories is automatically used in the AWR Design Environment platform WITHOUT the need to edit files in the installation folders.

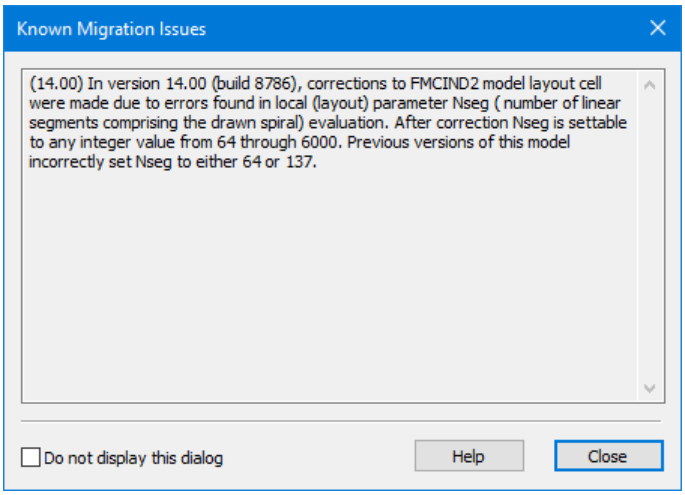
  The best way to migrate these libraries is to open your current *lib.xml* and *sys_lib.xml* files in the *Library* folder of your old installation and search for any paths you added to this library (perhaps compare with AWR Design Environment platform V15). Find those libraries and move the top level XML file to the directory listed above to break the cycle of needing to edit these installed XML files.

Other Concerns

Model Compatibility

TARGET: Designers

- When model changes are identified, the project can use a model compatibility flag. When you open an old project in a newer version of the AWR Design Environment platform software, the simulation results from the previous version do not change. You can change the model compatibility setting to see simulation results with the old and new model implementation. A dialog box similar to the following displays when you open your design in a newer version of the software if there are models with a compatibility setting in your design.



You can switch between model versions in the Circuit Options dialog box by choosing **Options > Default Circuit Options**, then clicking the **AWR Sim** tab, clicking the **Show Secondary** button, and then selecting the desired modeling version in **Model compatibility version**.

Multiple AWR Design Environment Software Versions

TARGET: AWR software installers

- Most users keep AWR Design Environment platform V16 software installed when upgrading to AWR Design Environment platform V22.1 to ensure their designs upgrade properly before converting permanently to the latest version.
- When you install AWR Design Environment platform V22.1 software, both versions run. Uninstalling any version may result in registry problems; therefore, when you uninstall, Cadence recommends that you also repair your active installation. One way to repair your installation is to open the Control Panel and then click on the Apps group. Under Apps & features, locate your AWR Design Environment platform installation and select it. Click the **Modify** button to display a dialog box with options for repairing or uninstalling the software. Select the **Repair/Modify** option and follow the prompts.

Redirection

TARGET: Users of any type of file redirection (changing the default location of any of the folders used by the AWR Design Environment platform)

- In networked environments, some users may choose to change the default location for certain files.
- Complete information on redirection is available in the *AWR Design Environment Installation Guide* under "Configuring Program File Locations". If you use this capability, ensure that you make the same changes in AWR Design Environment platform V22.1 software that you set up for AWR Design Environment platform V16.