cadence®

What's New in AWR Design Environment v16

Product Version 16

What's New in AWR Design Environment v16

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AWR Design Environment V16 What's New

What's New Organization

The Cadence® AWR Design Environment® V16 What's New document is organized into several sections:

- "*AWR Design Environment Features*" - Common improvements to all products.
- "*AWR Microwave Office Features*" - Cadence® AWR Microwave Office design-specific software improvements.
- "*AWR VSS (VSS) Features*" - Cadence® AWR® Visual System Simulator™ (VSS) communications and radar systems design-specific software improvements.
- "*Migration Issues*" - Migration issues from previous versions to the current version.

Features listed in this document may also include links to videos or reference examples included in the AWR Design Environment platform installation. Examples are listed by file name, for example: *filename.emp*. To find an example in the AWR Design Environment platform, choose **File > Open Example** and type the example name.

Major Features Overview

Limited Release Features

The current release includes some "Limited Release" features. In an effort to get customer feedback on features we are developing, and to ensure that those features are successfully solving the full range of the intended real-world engineering problems, Cadence® is releasing select features in this "Limited Release" state. These features, while in the software, may require a license to access. To use these features please contact your local Cadence Sales representative to obtain documentation and the appropriate license(s). Cadence strongly encourages you to provide feedback to ensure that these features work well and solve your engineering problems.

AWR Design Environment

- "Improved Python Interface": AWR Design Environment API intelligent code completion.
- "Version Control Integration": Enables large group design projects by managing AWR Design Environment documents with version control software.

AWR Microwave Office

- "Dynamic Voiding, Smoothing, and Automatic Net Connectivity Extraction": New layout modes and tools that facilitate net management on large designs.
- "Robust Simplex Optimizers": Enhanced Simplex optimizers with variable step size.
- "Multi-Version Process Library (PDK) Support": Use multiple version of a PDK in the same project.
- "Job Scheduler Enhancements": Support for multiple remote queues and per EM document remote queues.
- "Parallel and Remote Circuit Simulation": Run long circuit simulation or optimization jobs in parallel, either locally or remotely.
- "Interoperability with Allegro and Virtuoso Platforms": Create and analyze RF/microwave IP in AWR Microwave Office and share schematic and layout with Virtuoso and Allegro platforms. This is a limited release feature.
- "Remote Linux EM Simulations": Run a remote Cadence® AWR® AXIEM® 3D planar EM or Cadence® AWR® Analyst™ 3D FEM EM software simulation on a Linux LSF cluster.

- "AWR AXIEM Data Set Size Reduction": Exclude de-embedding network data from data sets.
- "Analyst Simulator Improvements": Various solver improvements.
- "Clarity 3D Solver Integration": Integration of the Cadence® Clarity™ 3D Solver enables direct simulation of 3D EM structures from within the AWR Design Environment platform. This is a limited release feature.
- "Celsius Thermal Solver Integration": Run thermal analysis directly on structures created in the AWR Design Environment platform. This is a limited release feature.

AWR VSS

- "Layout Trace Interconnect Modeling ": Model linear interconnects in AWR VSS.
- "RF Amplifier Power Saturation Improvements": Improved modeling of RF amplifiers operating in saturation.
- "Frequency Multiplier Amplitude and Spur Level Improvements": Improved modeling of RF multipliers operating in saturation.
- "APSK Modulation": Support for generic and DVB-S2 and CCSDS communication standards.
- "New LDPC Encoding Schemes": Support for LDPC codes used in 5G NR (NSA and SA), DVB-S2, Wireless LAN, and other standards .

AWR Design Environment V16 Licensing and Operating System Changes

See "Licensing Changes" for licensing and OS migration details.

AWR Design Environment Features

The Cadence® AWR Design Environment® V16 software includes the following new features, enhancements, and user interface changes. These changes are common to the Cadence® AWR® Microwave Office® software and Cadence® Visual System Simulator™ (VSS) communications and radar systems design software.

Improved Python Interface

A new pyawr library enables faster and less error prone scripting in Python. It incorporates win32com and adds AWR software-specific API functionality. Some of the features that pyawr provides include:

- Code-completion showing lists of API methods and variables associated with a particular API function
- Code-completion description and tips for the methods and variables
- Vector and array indexing that complies with Python coding conventions
- Descriptive error messages

Additional Information:

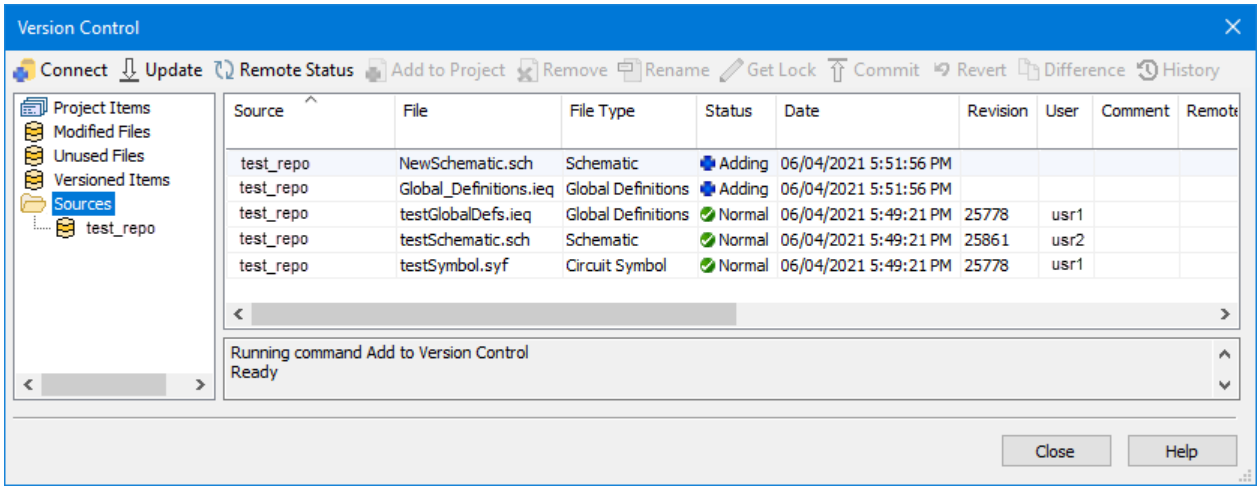
- Knowledge Base: Python.

Version Control Integration

The AWR Design Environment platform now supports integration of version control software to effectively manage group design of complex, multi-function projects on many different technologies. Use version control to easily collaborate between multiple designers and keep revision history of design data. Supported document types include:

- Global definitions
- Data files
- System diagrams
- Circuit schematics
- EM structures
- Netlists
- Circuit symbols
- Cell libraries (GDS and DXF)

Version control enhancements include hierarchy management. When adding/committing a hierarchical document, a second dialog box displays a list of dependent items that you can add to version control.



Additional Information:

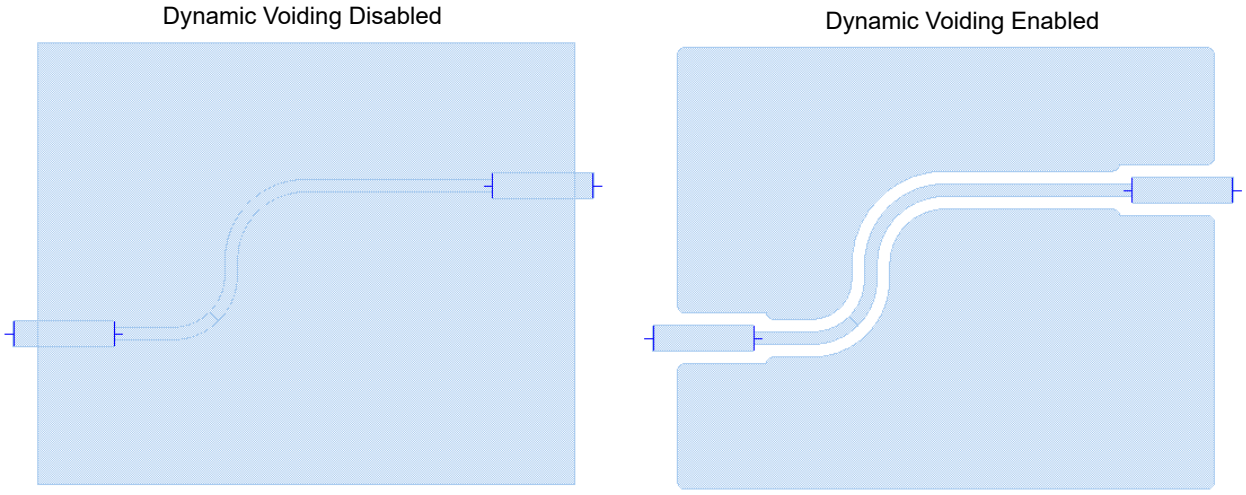
- Documentation: "Using Version Control".

AWR Microwave Office Features

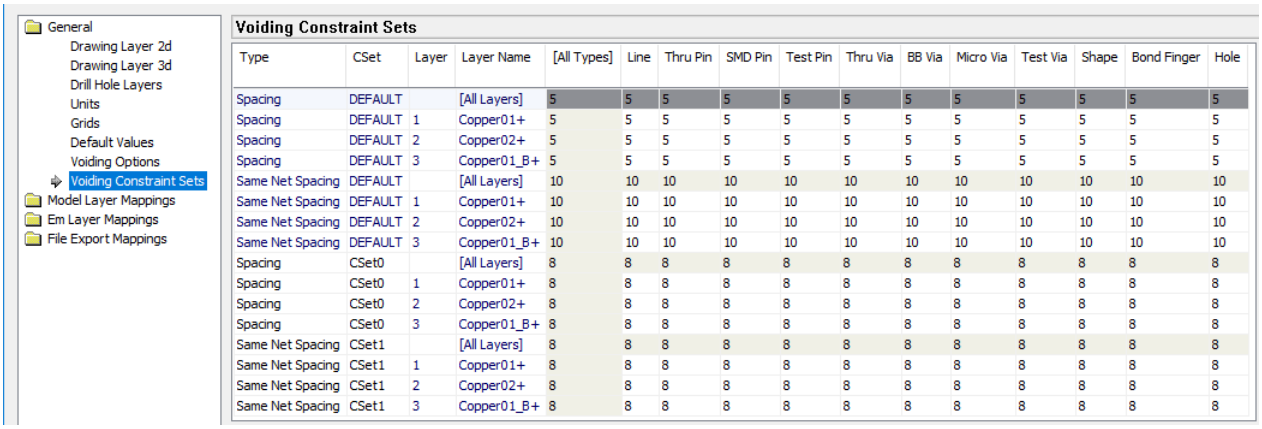
Cadence® AWR® Microwave Office® software V16 includes the following new features, enhancements, and user interface changes. The Cadence® AWR Design Environment® platform changes also apply to these specific products.

Dynamic Voiding, Smoothing, and Automatic Net Connectivity Extraction

A new dynamic voiding layout mode automatically analyzes the layout and generates the clearance between layout shapes and nets. For RF PCB applications, you can dynamically generate ground floods using Allegro-based voiding and smoothing algorithms, and easily run EM analysis on the voided and smoothed layout within the AWR Design Environment platform.



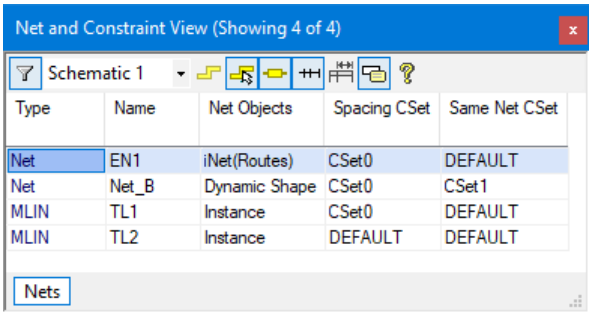
The clearance spacing between layout shapes and nets for various drawing layers is defined by constraint rules specified in the layout process file (LPF).



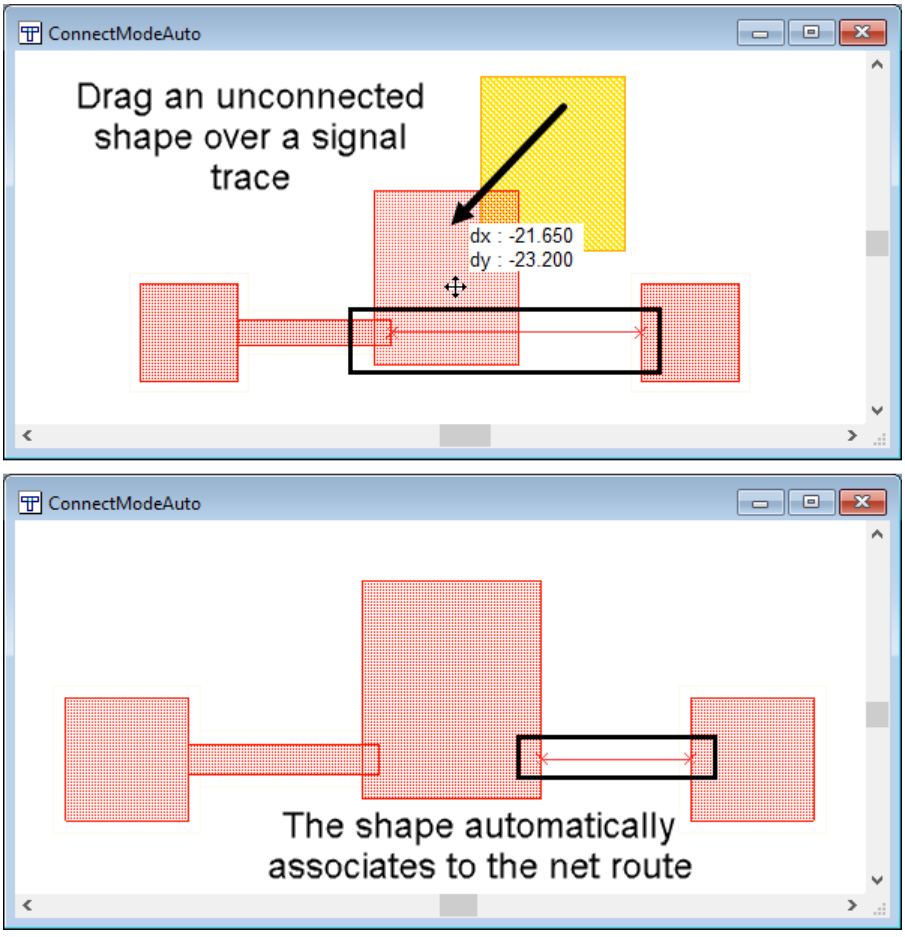
Type	CSet	Layer	Layer Name	[All Types]	Line	Thru Pin	SMD Pin	Test Pin	Thru Via	BB Via	Micro Via	Test Via	Shape	Bond Finger	Hole
Spacing	DEFAULT		[All Layers]	5	5	5	5	5	5	5	5	5	5	5	5
Spacing	DEFAULT	1	Copper01+	5	5	5	5	5	5	5	5	5	5	5	5
Spacing	DEFAULT	2	Copper02+	5	5	5	5	5	5	5	5	5	5	5	5
Spacing	DEFAULT	3	Copper01_B+	5	5	5	5	5	5	5	5	5	5	5	5
Same Net Spacing	DEFAULT		[All Layers]	10	10	10	10	10	10	10	10	10	10	10	10
Same Net Spacing	DEFAULT	1	Copper01+	10	10	10	10	10	10	10	10	10	10	10	10
Same Net Spacing	DEFAULT	2	Copper02+	10	10	10	10	10	10	10	10	10	10	10	10
Same Net Spacing	DEFAULT	3	Copper01_B+	10	10	10	10	10	10	10	10	10	10	10	10
Spacing	CSet0		[All Layers]	8	8	8	8	8	8	8	8	8	8	8	8
Spacing	CSet0	1	Copper01+	8	8	8	8	8	8	8	8	8	8	8	8
Spacing	CSet0	2	Copper02+	8	8	8	8	8	8	8	8	8	8	8	8
Spacing	CSet0	3	Copper01_B+	8	8	8	8	8	8	8	8	8	8	8	8
Same Net Spacing	CSet1		[All Layers]	8	8	8	8	8	8	8	8	8	8	8	8
Same Net Spacing	CSet1	1	Copper01+	8	8	8	8	8	8	8	8	8	8	8	8
Same Net Spacing	CSet1	2	Copper02+	8	8	8	8	8	8	8	8	8	8	8	8
Same Net Spacing	CSet1	3	Copper01_B+	8	8	8	8	8	8	8	8	8	8	8	8

The new Net and Constraint View window allows you to easily manage nets. You can quickly browse and filter among the various net objects in the selected schematic. You can assign net names and constraint sets to signal traces and

dynamic shapes for use in dynamic voiding. Additionally, you can highlight in both the Schematic and Layout Views instances and shapes associated with a selected net.



A new automatic net connectivity mode eliminates the need to manually select and associate shapes with nets. Shapes that overlay signal traces automatically inherit the net name of the signal trace.



Additional Information:

- Documentation: "Dynamic Voiding".

Robust Simplex Optimizers

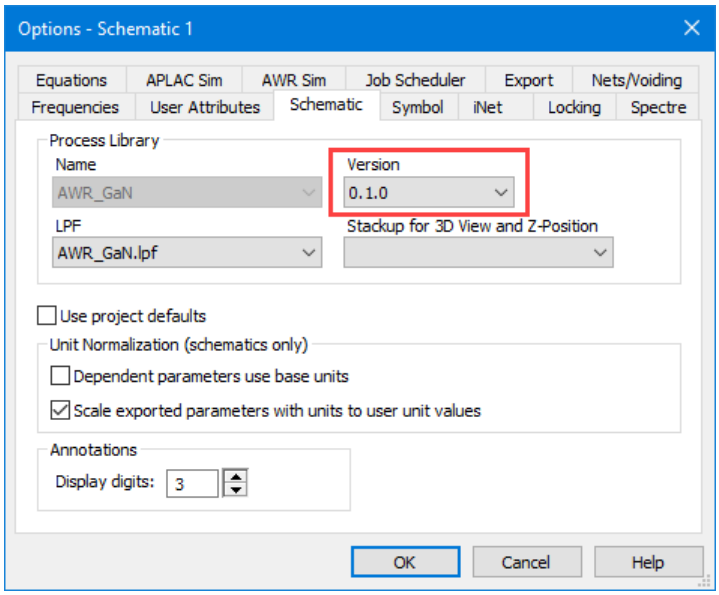
A new single-thread Robust Simplex optimizer and a Parallel Robust Simplex optimizer are introduced in this release. The new optimizers have an improved algorithm and are more flexible than current Simplex optimizers. They are more widely applicable and/or resistant to local minima. The parallel version can more thoroughly search the design space, therefore is even more robust to local minima.

Additional Information:

- Documentation: "Optimization Methods".

Multi-Version Process Library (PDK) Support

You can now design and simulate complex RF systems with IP from multiple versions of the same PDK within the same project. Global Definitions and LPF associations automatically update when changing PDK versions.

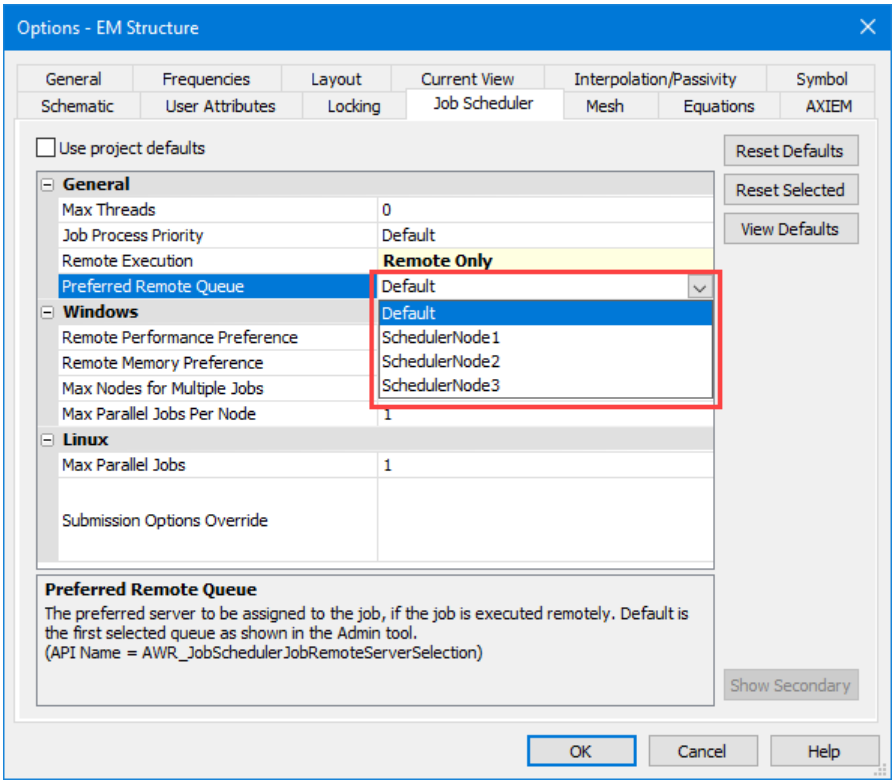


Additional Information:

- Documentation: "Working With Foundry Libraries".

Job Scheduler Enhancements

The Job Scheduler now supports enabling multiple remote queues simultaneously. Additionally, EM structures now support per-document remote queue selection. Possible setups include separate queues for Windows and Linux jobs, or separate Linux queues with different submit options.

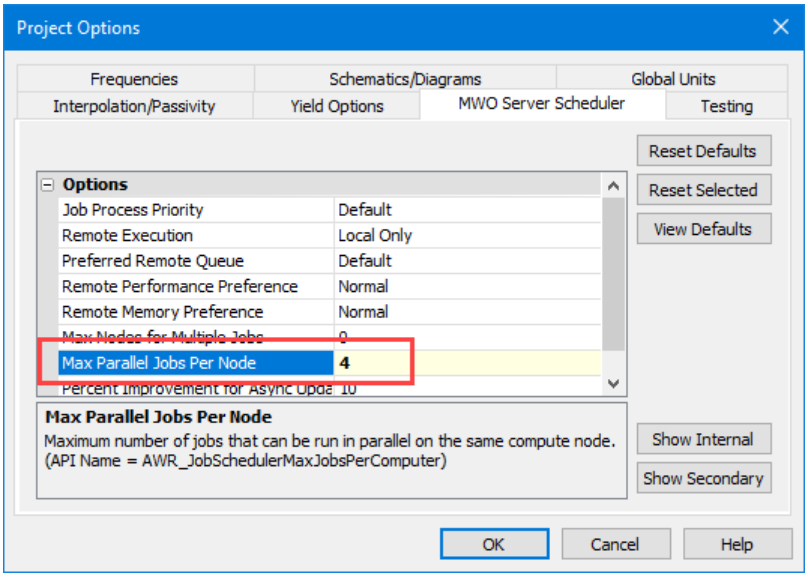


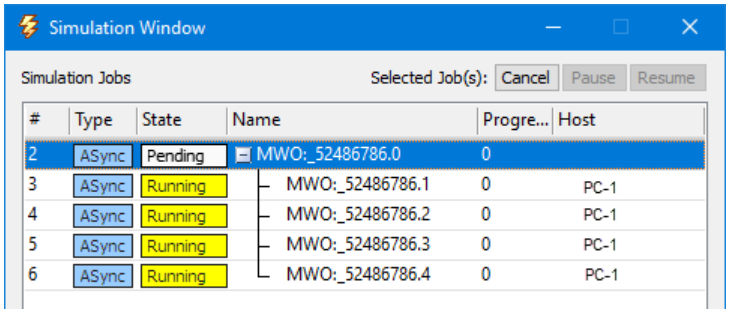
Additional Information:

- Documentation: "Utilizing Remote Computing".

Parallel and Remote Circuit Simulation

Parallel and remote circuit simulation enables multiple AWR Microwave Office software simulations to run simultaneously on the same computer, or remotely in parallel on multiple computers in a simulation queue. Long simulations, such as complex harmonic balance simulations, linear simulations involving extremely large S-parameters, parameter sweeps, load pull simulations, optimization, and yield analysis may benefit from a significant reduction in simulation time when run in parallel.



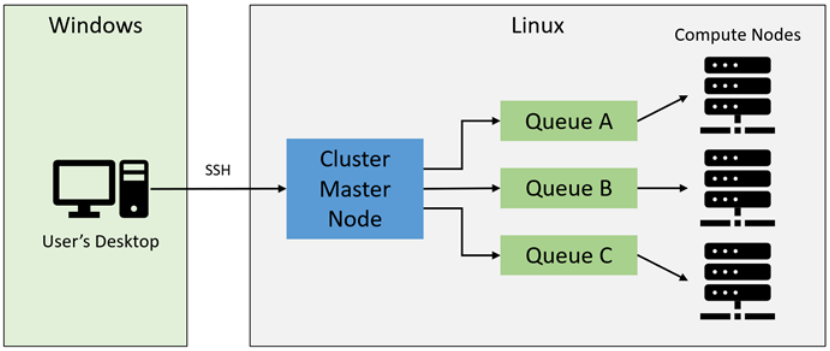


Additional Information:

- Documentation: "*Remote and Parallel Simulation* ".

Remote Linux EM Simulations

You can now run AWR AXIEM and Analyst simulations from the AWR Design Environment platform on a remote Linux cluster.

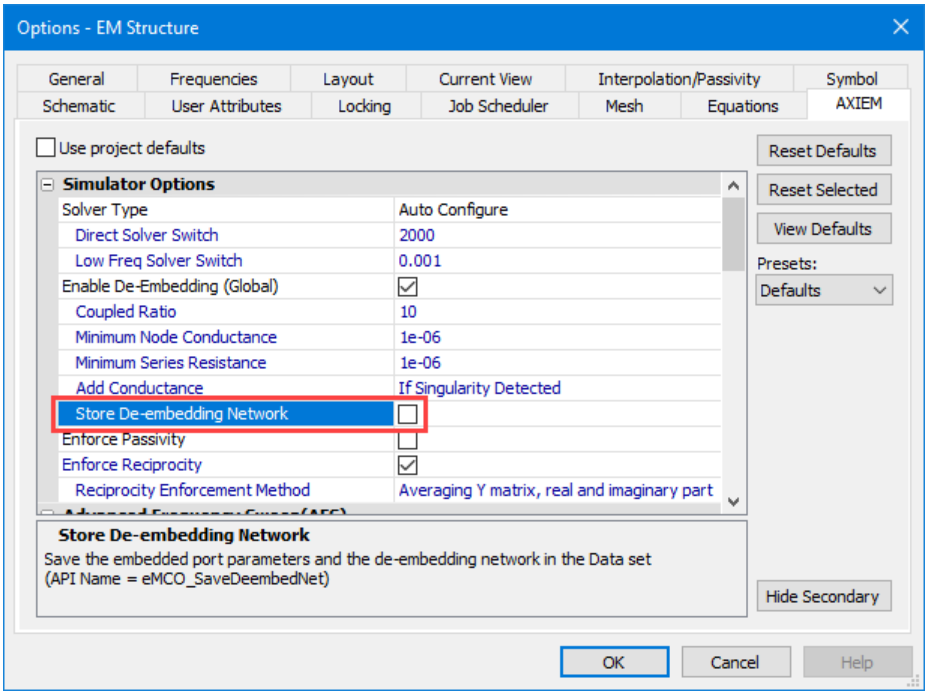


Additional Information:

- Documentation: "Remote Linux Simulations".

AWR AXIEM Data Set Size Reduction

A new **Store De-embedding Network** option allows you to choose whether to include or exclude EM structure de-embedding network data in the simulation data set. By default, the de-embedding network data is excluded, which can result in significant savings in the simulation data set size. Reduced data sets save hard disk space and improve data transfer performance with remote simulations.



Additional Information:

- Documentation: "Port De-embedding".

Analyst Simulator Improvements

Cadence® AWR® Analyst™ 3D FEM EM simulator improvements include:

- The Port Solver **Basis Set** secondary option is removed. The basis set used in the wave port solver is now always increased by one order.
- The choices for AMR Phase 1 (Ports Only) and AMR Phase 2 (Full Solve) **Frequency Modifier** secondary options are expanded to include **Mid/High** and **Low/Mid/High**.
- Improved support for multiple terminal configurations in wave ports, including stability and support for multiple positive terminals.

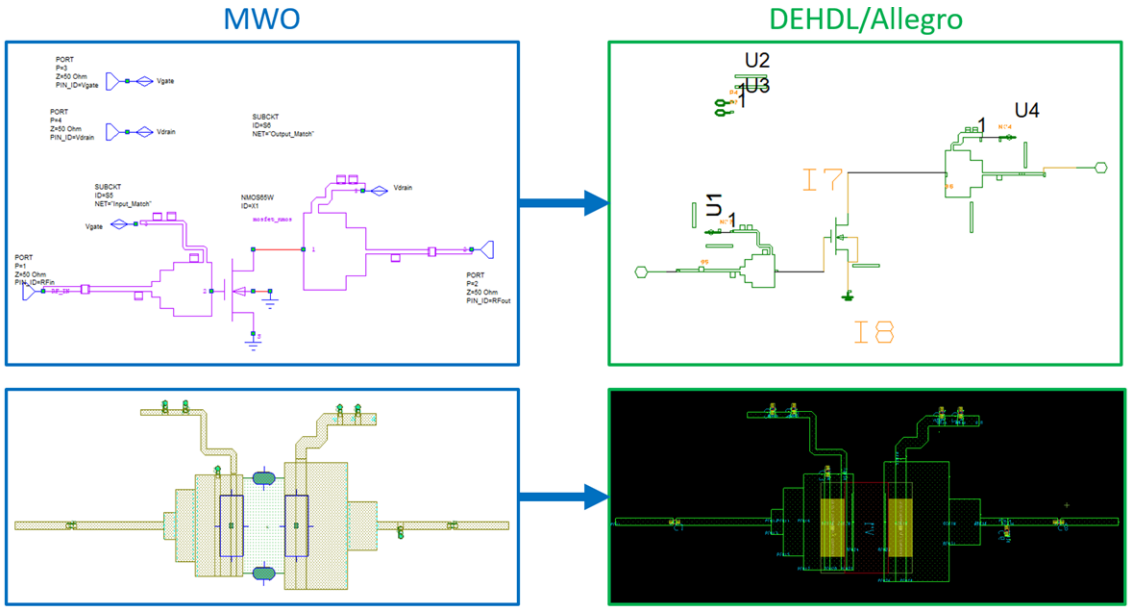
Interoperability with Allegro and Virtuoso Platforms

The AWR Design Environment platform now offers an RF/microwave design creation environment with import and export functionality to provide a pathway to and from Cadence® Allegro® PCB design tools and an export pathway to

Cadence® Virtuoso® Schematic Editor and Cadence® Virtuoso® Layout Suite. You can now create and analyze RF/microwave IP in AWR Microwave Office software, with the schematic and layout shared with Allegro/DE-HDL, and Virtuoso software. Interoperability between these software tools facilitates the design and analysis of RF/microwave, analog, and digital design elements together.

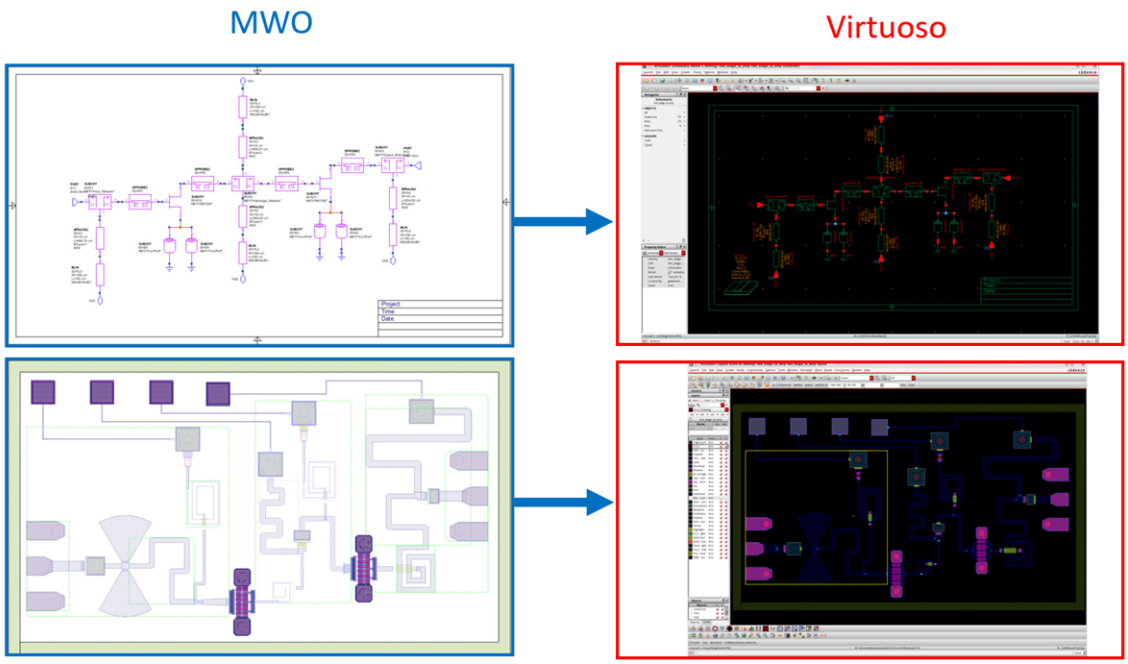
The foundation for interoperability is the Unified Library. Unified Libraries are common databases that AWR Microwave Office, Allegro/DE-HDL, and Virtuoso software can read. They contain the technology, component, and design information required to properly analyze, verify, and manufacture a design.

NOTE: This is a limited release feature.



Additional Information:

- Documentation: "AWR Design Environment/Allegro Interoperability".

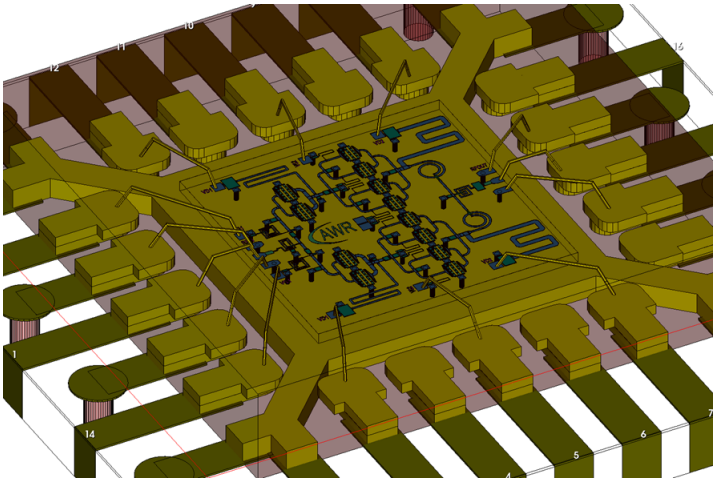


Additional Information:

- Documentation: "AWR Design Environment/Virtuoso Interoperability".

Clarity 3D Solver Integration

Simulate EM structures from within the AWR Design Environment platform using the Cadence® Clarity™ 3D Solver, a 3D full-wave electromagnetic (EM) simulation software tool. Clarity has the ability to solve much larger problems such as entire modules and complete BAW/SAW filters with greater speed.



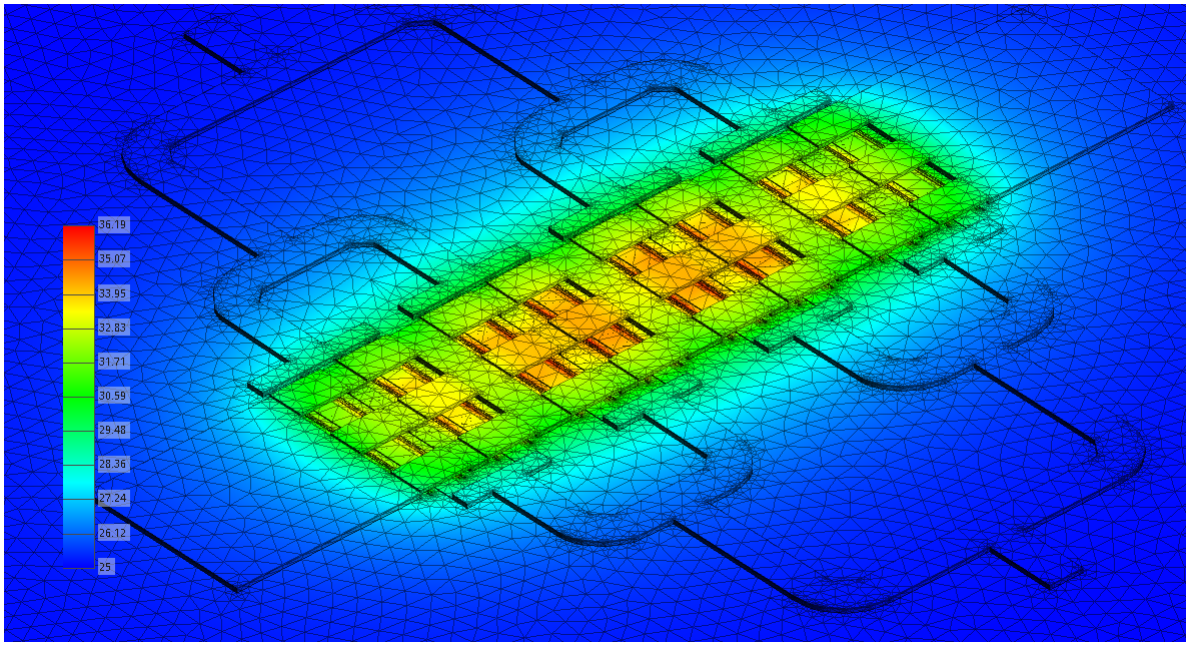
NOTE: This is a limited release feature.

Additional Information:

- Documentation: "Clarity 3D Solver".

Celsius Thermal Solver Integration

Run thermal analysis from within the AWR Design Environment platform using the The Cadence® Celsius™ Thermal Solver. You can create Celsius EM structures by either drawing the geometry in the EM editor, or by using EM extraction. After simulating, open the structure in the Celsius native editor to view 3D field plots of the thermal temperature distribution. Temperature results of the Celsius simulation are returned to the AWR Design Environment platform.



NOTE: This is a limited release feature.

Additional Information:

- Documentation: "Celsius Thermal Solver".

Minor Improvements

AWR Microwave Office V16 software includes the following minor new features, enhancements, and user interface changes.

New Circuit Models

The following new circuit models are included in AWR Microwave Office v16 software.

Coplanar Elements

- "Coplanar Waveguide Interdigital Capacitor (Aggregate): CPWICAP"
- "Rectangular CPW Inductor with AirBridge/Underpass (EM Quasi-Static): CPWRINDB"
- "CPW Thin Film Resistor for MMIC (Closed Form): CPWTFRM"
- "2 Asymmetric Coupled Coplanar Lines on Multilayer Substrate (EM Quasi-Static): GCPW2LNA"

- "Lower CPW Broadside Coupled to Upper Microstrip Line on Multilayer Substrate (EM Quasi-Static): GCPWBCGD"
- "2 Asymmetric Broadside Coupled Coplanar Lines on Multilayer Substrate (EM Quasi-Static): GCPWBCGG"
- "Upper CPW Broadside Coupled to Lower Microstrip Line on Multilayer Substrate (EM Quasi-Static): GCPWBCGU"
- "Coplanar Asymmetric Line on Multilayer Substrate (EM Quasi-Static): GCPWALIN"

Microstrip Components

- "Microstrip Interdigital Capacitor on Multilayer Substrate (Aggregate): MMICAP"
- "Tapered Microstrip Line on Multilayer Substrate (EM Quasi-Static): MMTAPER"
- "Tapered Microstrip Line Synthesized to Match (Klopfenstein, Exponential, Triangular): MTAPER2"
- "Microstrip Radial Stub Series on Multilayer Substrate (EM Quasi-Static): MMRSTUB"
- "Microstrip Radial Stub Shunt on Multilayer Substrate (EM Quasi-Static): MMSRSTUB"
- "Microstrip Lange Coupler with Optional Cover(EM Quasi-Static): MLANGE2C"

Interconnects and Lumped Elements

- "Multilevel Bond Wire Model (User-defined Multisegment Shapes with Varying Number of Segments): BWIRES4"
- "Mutually Coupled Coils: N Inductors (Closed Form): MUCN"

New Circuit Measurements

The following new circuit measurements/annotations are included in AWR Microwave Office V16 software.

Linear Measurements

- "Transmission Line Characteristics and RLGC Parameters: TxPar "

Output File Measurements

- "Write Total Power for All Elements to File: TOT_PWRF"

API

- API access is added to the DesignRuleChecker.ErrorWindow.Title which enables customization of the Error Window title.

Cell Libraries

- Improved performance of copying cells in large Cell Libraries.

Graphs

- The symbols drawn for single-point optimization/yield goals on graphs now make it clear what type of goal is represented.
- Graphs with measurements using **All Sources** as the data source now correctly update to include newly added data sources when XML Library elements based upon Touchstone and MDIF data files are brought in to a project.

Job Scheduler

- The Job Scheduler now starts asynchronously when the AWR Design Environment platform starts, allowing faster initial simulations and enabling the Job Monitor to fetch data sets without requiring an initial simulation.
- Saving changes to a remote host in the Job Scheduler Admin tool now causes the host connection to reset and reconnect with the new parameters so that restarting the running Job Scheduler is no longer necessary to pick up the changes. This improvement applies to both Windows and Linux remote hosts.

Layout

- Fixed a layout performance issue when the Layout Editor Mode option **Draw route vias as X** is selected.

Layout - EM

- When setting the Z-position of a subcircuit, the drop-down list now displays the dielectrics in descending order from top to bottom. The dielectric name now displays next to the index to aid in layer selection.

Output Equations

- Implemented the **Draw border on window** option in the Properties dialog box for Window-in-window views in Output Equations documents.

Schematic Editor

- When pushing into a SUBCKT using the **Edit Subcircuit** command, you can now choose which Switch View document to push into when available.

Simulation - APLAC

- Added AC analysis support for several ports, including PORT_PS1. For PORT_PS2, an AC source is only added to the 1st tone.
- Noise is now simulated whenever there is an active NPORTF output file measurement for a 2-port and the Write Noise for Active Source parameter is selected.

User Interface

- You can now **Shift-** double-click on a schematic node in the Project Browser to open the Layout View of the schematic.
- Increased the column width of the **#** column in the Simulation window so that job numbers greater than two digits properly display.
- Rich text boxes now support fill translucency.
- Pressing the **Shift** key while dragging and dropping a file (such as a schematic, netlist, or data file) from Windows Explorer into the AWR Design Environment platform will link the file instead of embedding it.
- Updated the drag and drop mechanism to accept all the files that can be linked to, including Global Definitions and circuit symbol files.
- Dialog boxes that support column filtering, such as the Open Example Project dialog box, now have filtering functionality by default.

AWR VSS (VSS) Features

The Cadence® AWR® Visual System Simulator™ (VSS) communications and radar systems design V16 software includes the following new features, enhancements, and user interface changes. The Cadence® AWR Design Environment® platform changes also apply to this product.

Layout Trace Interconnect Modeling

The new INTRCONN block models the effects of transmission line loss, impedance mismatch, and coupling. This block has five different operating modes to facilitate budget analysis with a design flow that begins with rough estimates of the layout, progressing to using final PCB layout traces in an EM simulation. The operating modes include:

- Attenuator: The INTRCONN block functions as the AWR VSS RFATTEN block for early estimation of PCB traces where trace loss and mismatch effects can be modeled.
- Microstrip: This mode uses the same model as the AWR Microwave Office MLIN element. More refined PCB trace effects can be modeled that use physical parameters of both the microstrip trace and the PCB substrate.
- Linear co-simulation (LIN_S): The INTRCONN block functions as the AWR VSS LIN_S block. This allows linear co-simulation with an AWR Microwave Office circuit or a Touchstone data file. This is another level of PCB trace modeling refinement where the PCB trace can be modeled with more complex circuit designs, other transmission line types such as stripline, coplanar waveguide, and others. Additionally, the PCB trace data can come from an EM structure.
- Coupling co-simulation: The INTRCONN block functions as the AWR VSS LIN_S block, but with added capability that includes coupling between multiple PCB traces.

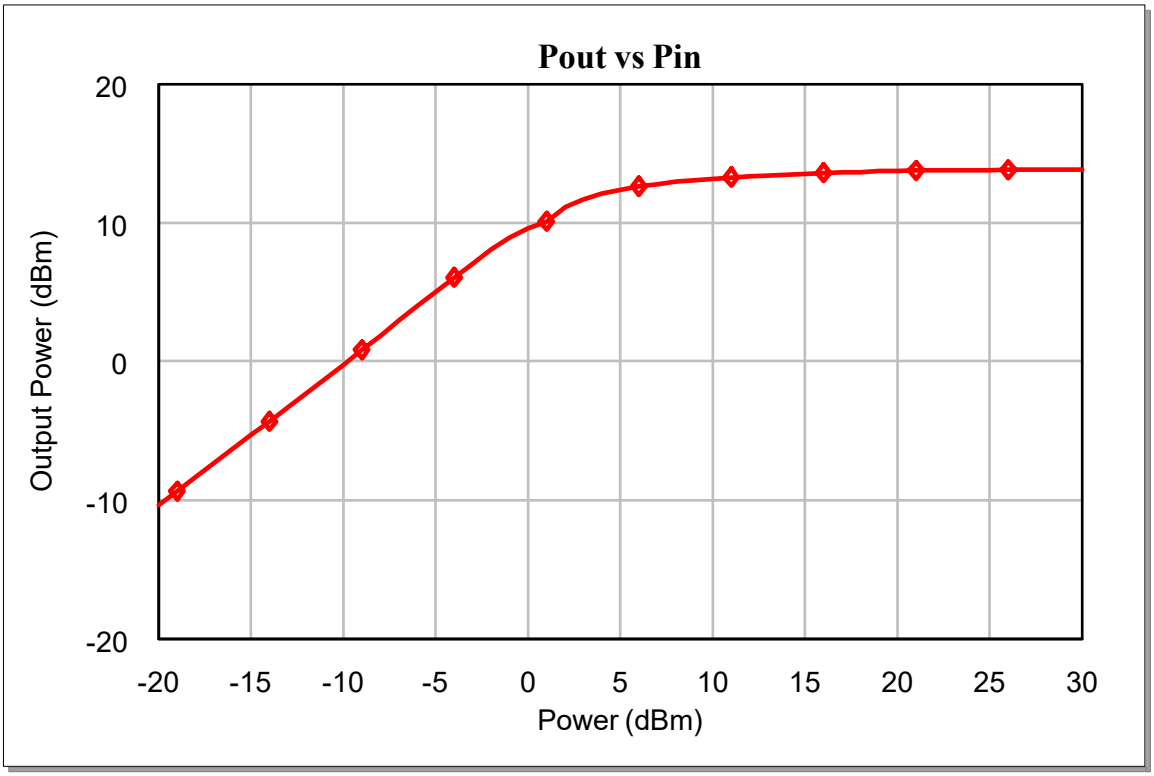
Design efficiency is greatly enhanced in that a single block in the system diagram can be used for multiple purposes. For coupling mode, multiple input frequencies are supported whereas only a single frequency is supported when using LIN_S for trace coupling co-simulation. An additional coupling feature is that frequency-dependent impedance mismatch and frequency-dependent coupling can be based on circuit or EM co-simulation as opposed to the SCOUPLING block where the coupling is parameter-based and frequency-dependent impedance mismatch is not supported.

Additional Information:

- Documentation: “Interconnect: INTRCONN”.
- Example: *Interconnects_Design_Flow.emp*

RF Amplifier Power Saturation Improvements

Improvements to the behavioural modeling of RF amplifiers close to or in saturation now yields a smoother power output versus power input curve. These improvements apply to time domain, RF Budget Analysis, and RF Inspector simulations. When input power to the amplifier is high enough to drive the amplifier into saturation, the output power is modeled as a clipped sine wave when driven with a sinusoid. The saturated output power level and the output spectrum remain constant as a function of input power level.



The following models have improved power saturation modeling:

- "Behavioral Amplifier: AMP_B"
- "Behavioral Amplifier, 2nd Generation: AMP_B2"
- "Behavioral Amplifier (Voltage-Based): AMP_BV"
- "Equation-based Nonlinear Amplifier: AMP_EQN"
- "Frequency Dependent Behavioral Amplifier (File-Based): AMP_F"
- "MDIF File Based Nonlinear Behavioral Model: NL_MDIF"
- "Nonlinear Behavioral Model (Simulation-Based): NL_S"
- "Nonlinear Variable Gain Amplifier (File-Based): VGA_F"

Frequency Multiplier Amplitude and Spur Level Improvements

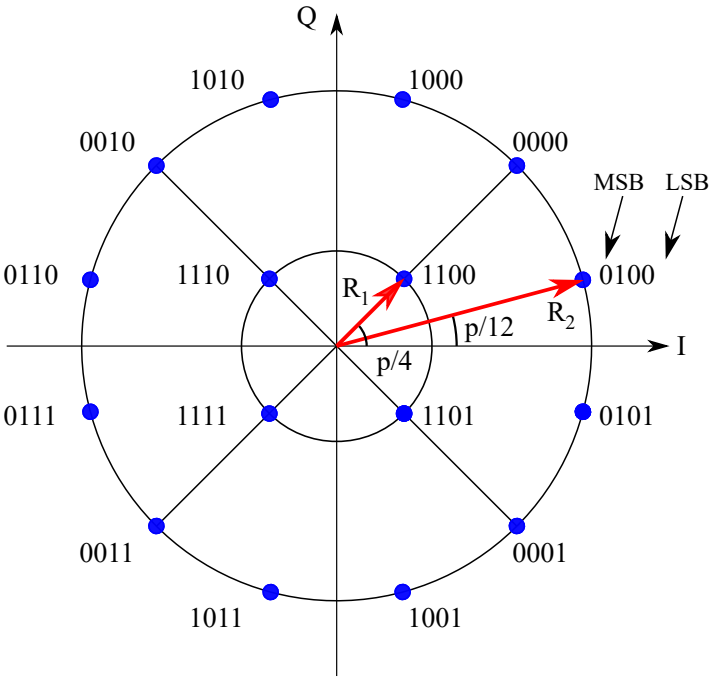
The behavioral modeling of RF frequency multipliers is improved for both saturated output power and spur level. The improvements pertain to the following AWR VSS blocks:

- "Behavioral Frequency Multiplier: FMULT_B "
- "Behavioral Frequency Multiplier, 2nd Generation: FMULT_B2 "

These improvements yield close agreement in saturated output power and spur level between time domain, RF Budget Analysis, and RF Inspector simulations. The predicted performance is less sensitive to input power variation, matching the behavior of physical frequency multiplier devices.

APSK Modulation

APSK modulations are used, among others, in DVB-S2 and CCSDS communication systems. AWR VSS V16 adds support for the APSK modulations defined in section 5.2.3 of the CCSDS specifications, and in sections 5.4.3 and 5.4.4 of the DVB-S2 specifications. In addition, you may define custom APSK modulation schemes. AWR VSS offers both modulation and demodulation functionality.



New LDPC Encoding Schemes

Various forms of LDPC (Low Density Parity Check) codes are used in several modern communication standards such as 5G NR (NSA and SA), DVB-S2, Wireless LAN, and others. AWR VSS V16 includes the variants used in the CCSDS 131.0-B-3 standard and supports coding rates 1/2, 2/3, 4/5 and ~7/8 (223/255), and the corresponding block sizes. The encoder and decoder for this version of the LDPC code are included in AWR VSS V16.

Minor Improvements

AWR VSS V16 software includes the following minor new features, enhancements, and user interface changes:

New/Updated Examples

The following are new or updated AWR Design Environment platform examples. To find an example, choose **File > Open Example** and type the example name.

- *Interconnects_Design_Flow.emp*
- *LTE_DL_RX_TestBench.emp*
- *LTE_DL_TX_TestBench.emp*

- *LTE_UL_RX_TestBench.emp*
- *LTE_UL_TX_TestBench.emp*
- *NBIoT_Inband_UL_RX_TestBench.emp*

New/Updated System Blocks

The following new system blocks are included in AWR VSS V16 software.

Interconnects

- "Interconnect: INTRCONN"

Modulation

- "QAM Detector: APSK_DET"
- "APSK Mapper: APSK_MAP"
- "APSK Receiver: APSK_RX"
- "APSK Soft Metrics Calculator: APSK_SFTM"
- "APSK Modulated Signal: APSK_SRC"
- "APSK Transmitter: APSK_TX"

Simulation Control

- "RFB Thermal Noise Simulation Control: RFBTNSCTL"

New System Measurements

The following new system measurements are included in AWR VSS V16 software.

RF Budget Measurements

- "Cascaded VSWR: C_VSWR "

System Eye Diagram Measurements

- "Eye Histogram: EYE_HIST "

Measurements

- The C_HDRM measurement now takes into account all incoming signals at the signal frequency. Previously, it only measured the primary signal, ignoring any coupled signals at the same frequency.

Simulation

- The built-in variable _FREQ is now available to all AWR VSS simulators. For RF Budget Analysis simulations, _FREQ is set to an array containing all the frequencies from the System Simulator Options dialog box **RF Frequencies** tab. Previously, these values were only available to RF Budget Analysis simulations if the system diagram contained PORT_SRC blocks. For RF Inspector and Time Domain simulations, _FREQ is set to only the first frequency value from the **RF Frequencies** tab. This reflects the fact that RF Inspector and Time Domain simulations do not use the frequencies from the **RF Frequencies** tab and are therefore not swept by those frequencies.

- The propagated noise PSD property, which is reported by the NOISEPSD annotation and the NOISE_PROP measurement, now includes feed-through noise from the LO. The NOISEPSD measurement now also more reliably reports the noise when set to "Spot Noise PSD at fc". Previously, it only reported the first noise value.
- The new RF Budget Analysis Thermal Noise Simulation Control, RFBTNSCTL, allows for the finer specification of noise frequency offsets for RF Budget Analysis noise measurements that utilize a range of frequencies, such as C_PHS_NOISE when operating with a thermal noise floor, C_SNR, and SFDR_RFB.

  C_PHS_NOISE handling of the thermal noise floor now supports these frequencies. However, C_PHS_NOISE with thermal noise floor applied no longer supports specifying multiple frequencies on the System Simulation Options dialog box **RF Frequencies** tab.

  C_PHS_NOISE now includes additional display options for displaying the thermal noise floor without the phase noise.

  See Noise Modeling in AWR VSS for more information on these changes.
- The algorithm used in RF Budget Analysis simulations to select the signal path among branched paths is updated to make paths through the OFF state of RF switches more expensive, and hence less likely to be chosen. Similar increases along other isolated paths were also made to make those paths less likely to be chosen.

System Block Updates

- To better condition frequency-dependent impedance mismatch results, RF_START and RF_START_NS now apply a very small loss of approximately -0.0000009 dB for S21 and a very small gain for S12 of -160 dB.
- The following issues with using the PLO parameter in the AWR VSS mixers are resolved:
  - When PLOUSE or PLOTYP is set to **Reference LO power** (formerly **Spur reference only**), the propagated signal power property now matches the output power under matched load conditions as the LO power is varied. Previously, the propagated signal power did not vary with LO power.
  - When PLOUSE or PLOTYP is set to **(Rarely used) LO power, LO input is normalized input** (formerly **LO port power**) the propagated signal power property now matches the output power under matched load conditions as the LO power is varied. The available gain reported by C_GA now also matches the power gain reported by C_GP under matched load conditions as the LO power is varied.
  - Note that you should only use the **(Rarely used) LO power, LO input is normalized input** (formerly **LO port power**) in very special cases. With this setting, the LO input signal is treated as a normalized signal. This means the mixer 'sees' an LO of power level PLO when the voltage on the LO input is 1 V.
- The AWR VSS Mixers blocks now apply any phase rotation on the LO to the propagated phase rotation at IF output to match the phase rotation that occurs with the IF signal. This allows the RCVR blocks to better detect the original signal when there is phase rotation on the LO signals.
- MIXER_S now includes phase shifts from the AWR Microwave Office schematic.
- The time domain generation of 2nd and 4th order harmonics in AMP_F is improved. The handling of 2nd and 4th order spurs in FMULT_B and FMULT_B2 for N ≤ x5 is also improved.
- The FMULT_B2 and FMULT_B blocks are significantly updated. The handling of PINCLIP is changed so that if both MEASREF/PIN and PINCLIP are specified, the blocks by default use a new saturation mode. This mode generates similar results for Time Domain, RF Budget Analysis, and RF Inspector simulations for a single tone input signal. The mode employs a narrowband model where higher order harmonics do not contribute to lower order harmonics, which differs from a straight polynomial based model. The result is the output from a single tone input signal is much more predictable over various input power levels.

  In addition, the RF Inspector narrowband modeling used for simulations with N higher than x5 is updated so each harmonic term only generates components around the harmonic term and does not contribute to lower order harmonics.

- LTE_FRMASM and LTE_FRMDSM now support TDD burst formats up to Rel.16 LTE. This includes mode selection for UL TDD or DL TDD, desired cyclic prefix mode, special subframe configurations (with options for additional SC-FDMA symbols in UpPTS), and Uplink-Downlink configuration for burst shaping within a transmission frame.
- The AWR VSS antennas now treat negative dB values for AXRATIO as a swapping of the major and minor axes of the polarization ellipse, adding 90-degrees to the polarization angle to account for the swap. This allows for a smooth transition through 0 dB when sweeping AXRATIO.
- The SCANLOSSN parameter is added to the PHARRAY_ANT model to simulate scan loss effect when using isotropic antenna elements. The parameter N is based on the common model cos^N(theta).
- A number of changes are made to the SCOUPLING block:
  - New C_I2MR and C_M2IR parameters are added to better control the coupling for the reverse directions (between ports 3 and 1, and between ports 4 and 2).
  - New ZM and ZI parameters are added to allow specification of the characteristic impedances of the main and interfering signal ports.
  - The insertion loss is increased to -0.001 dB to better condition the resulting Y matrices.

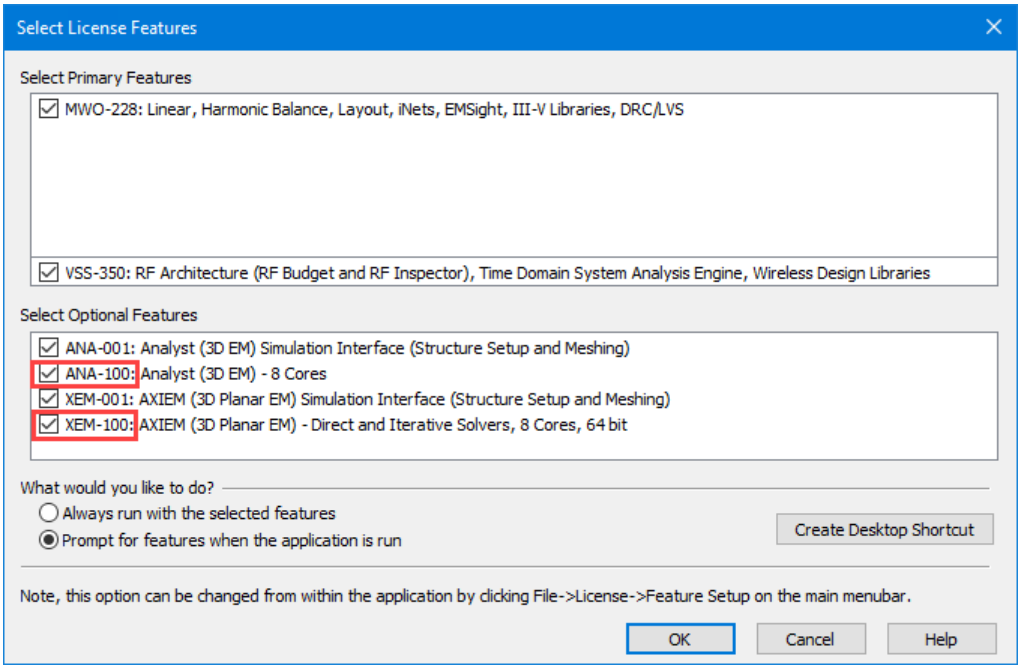
Migration Issues

The following are issues you need to address when migrating from a Cadence® AWR Design Environment® platform V15 release to an AWR Design Environment platform V16 release. Not all topics apply to every user. If you are not familiar with a topic or program feature included here, it probably does not apply to your use of the software. You should read about all of the issues before developing your migration strategy. The path to the <Appdatauser> files referenced in this document is operating system dependent. To view the directory path to your <Appdatauser> files, choose **Help > Show Files/Directories** to display the Directories dialog box, then double-click the *Appdatauser* folder.

AWR Design Environment V16 Specific Migration Issues

Licensing Changes

- XEM-100 and ANA-100 are now optional startup features. You must select them when launching the AWR Design Environment platform in order to run Cadence® AWR® AXIEM® 3D planar EM analysis or Cadence® AWR® Analyst™3D FEM EM analysis, and those features are held for the entire session. If you normally start the AWR Design Environment platform with a desktop shortcut that includes saved features, or have selected **Always run with the selected features** in the Select License Features dialog box, your saved features list may not include XEM-100 or ANA-100. In that case, you will have errors when trying to run AWR AXIEM or Analyst tool simulations. To fix the errors, you must recreate your desktop shortcut or startup list to include those features.



- Process Design Kits (PDKs) no longer require a separate feature in license files. If the foundry has granted access, you can use the PDK.

Operating System

The AWR Design Environment platform V16 software no longer supports Windows 8 and Windows Server 2012 operating systems.

AWR AXIEM Data Sets

Starting in the AWR Design Environment V16 platform , AWR AXIEM simulations no longer store de-embedding network data in the simulation data sets by default. This option reduces data set file size. Data sets generated in previous AWR Design Environment versions have de-embedding data stored in the data set. When you open older projects with data sets in the AWR Design Environment V16 platform, **Store De-embedding Network** is not selected by default, but a forced resimulation is still necessary to remove the de-embedding network data from the simulation data set. See "AWR AXIEM Data Set Size Reduction" for a summary.

Job Scheduler Remote Execution Options

The Job Scheduler remote execution options are reduced to two choices: **Local Only** or **Remote Only**. When opening older projects in AWR Design Environment platform V16 software, the eliminated **Prefer Local** setting now maps to **Local Only**, and the **Prefer Remote** and **Any Available** settings now map to **Remote Only**.

Process Libraries

In AWR Design Environment platform V16 software, you can now associate schematics with a process library. When an older project is loaded into V16 software, if the project uses a single process library, all schematics are automatically configured to use that library. If the project uses more than one library, the library settings for each schematic are based upon which LPF the schematic uses.

API

The element XmlBrowserPath and XmlComponentPath property (for example: ele.Properties("XmlBrowserPath").Value) is removed and replaced with direct methods (for example: ele.XmlBrowserPath).

The arc drawing function pCell API now honors the **Number of points/circle** layout option instead of using a hard-coded value of 72. The Arc drawing pCell API now matches the circle drawing pCell API.

Version-Independent Migration Issues

The items in this section address moving files and settings from one software version to another. Some of these files and settings are automatically migrated. If the previous software version is not found, up to three major versions back are searched. For example, if migrating to the AWR Design Environment platform V16, AWR Design Environment platform V15, AWR Design Environment platform V14, and AWR Design Environment platform V13 software are searched.

NOTE: Ensure that your Windows® Explorer program is set to show hidden and system files.

Files Automatically Migrated

The *Appdatauser* and *Appdatacommon* folders must be in their default locations for files or directories to auto-migrate. Changing their default locations would necessitate creating a *redirect.ini* file in the program directory, and is not a common practice.

Files in Appdatacommon

The migration of Appdatacommon is triggered based on the existence of the *mwoffice.ini* file in the *Appdatacommon* folder for the newly installed version.

- If there is an existing *mwoffice.ini* file, no files or folders are migrated.
- If the *mwoffice.ini* file does not exist, it is copied from the previous location if found.

- If the *mwoffice.ini* file does not exist and an older version is not found, a new file is created.

The path to each PDK is stored in the *mwoffice.ini* file and is available for any user of that computer. The installation location of foundry libraries is typically version-independent; the default installation locations are not dependent on the AWR Design Environment software version. These paths are used when opening a project using a PDK or by choosing **File > New with Library**.

All additional files and directories at this location are not copied since they should not be used with the new version of the software.

Files in Appdatauser

The migration of Appdatauser is triggered based on the existence of the *user.ini* file in the *Appdatauser* folder for the newly installed version. If there is an existing *user.ini* file, no files/folder are migrated. No existing files or folders are overwritten.

The following files/folders are migrated:

- All *.ini* files located at the top level directory of *Appdatauser*, including *user.ini*. The *user.ini* file contains environment settings, custom layout modes, and other environment defaults.
- All XML files located at the top level directory of *Appdatauser*. This includes:
  - *customizations.xml* - contains your hotkey settings.
  - *UICustomizations.xml* - contains your menu settings. You can reset the menus to the AWR Design Environment platform V15 defaults.
  - *UIDockingLayout.xml* - contains settings for how different windows are docked in the AWR Design Environment platform.
  - *UIToolBarLayout.xml* - contains your toolbar settings. You can reset the toolbars to the AWR Design Environment platform V15; defaults.
  - *materialdefs.xml* - There are several pre-set materials such as FR4, alumina, and GaAs available in the EM interface. If you modify these settings, the changes are stored in *materialdefs.xml*.
- These directories:
  - *scripts* - Global (available in any project) Visual Basic scripts.
  - *models/model64* - Custom models used in the AWR Design Environment platform.
  - *cells/cells64* - Custom cells used in the AWR Design Environment platform.
  - *symbols* - Custom symbol files created in the AWR Design Environment platform.
  - *em_models* - User-filled X-model tables.
  - *XML* - XML libraries installed in the default location.

All additional files and directories in this location are not copied since they should not be used with the new version of the software.

Files NOT Automatically Migrated

User-Defined XML Libraries

TARGET: Users who have local XML libraries (anything outside of the AWR web library)

- Many users either choose to install a local copy of the XML libraries or add to the default installation with other vendor-specific XML libraries. The default location is the <*Appdatauser*> folder. If your XML is in this location it can be migrated automatically (see "Files Automatically Migrated ").
- Starting in AWR Design Environment platform V11, the correct location for these libraries is *:\Users\UserName\AppData\Local\AWR\Design Environment\V11.0\XML*. There are top level folders for *3D EM Elements*, *Circuit Elements* and *System Blocks*. Any XML file located in these top level directories is automatically used in the AWR Design Environment platform WITHOUT the need to edit files in the installation folders.

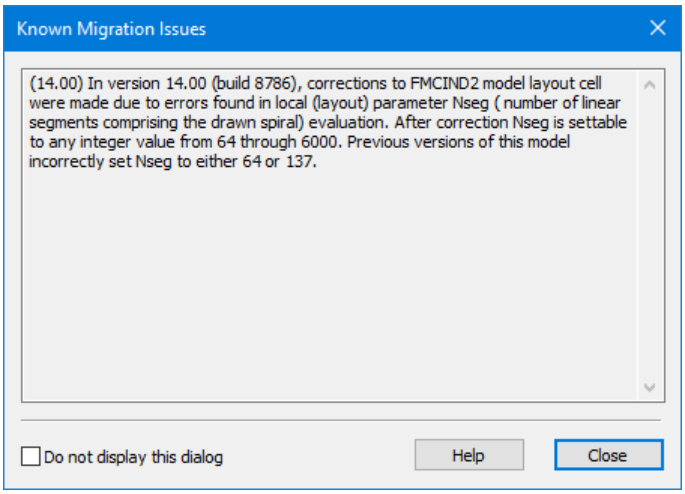
  The best way to migrate these libraries is to open your current *lib.xml* and *sys_lib.xml* files in the *Library* folder of your old installation and search for any paths you added to this library (perhaps compare with AWR Design Environment platform V15). Find those libraries and move the top level XML file to the directory listed above to break the cycle of needing to edit these installed XML files.

Other Concerns

Model Compatibility

TARGET: Designers

- When model changes are identified, the project can use a model compatibility flag. When you open an old project in a newer version of the AWR Design Environment platform software, the simulation results from the previous version do not change. You can change the model compatibility setting to see simulation results with the old and new model implementation. A dialog box similar to the following displays when you open your design in a newer version of the software if there are models with a compatibility setting in your design.



  You can switch between model versions in the Circuit Options dialog box by choosing **Options > Default Circuit Options**, then clicking the **AWR Sim** tab, clicking the **Show Secondary** button, and then selecting the desired modeling version in **Model compatibility version**.

Multiple AWR Design Environment Software Versions

TARGET: AWR software installers

- Most users keep AWR Design Environment platform V15 software installed when upgrading to AWR Design Environment platform V16 to ensure their designs upgrade properly before converting permanently to the latest version.

- When you install AWR Design Environment platform V16 software, both versions run. Uninstalling any version may result in registry problems; therefore, when you uninstall, Cadence recommends that you also repair your active installation. One way to repair your installation is to open the Control Panel and then click on the Apps group. Under Apps & features, locate your AWR Design Environment platform installation and select it. Click the **Modify** button to display a dialog box with options for repairing or uninstalling the software. Select the **Repair/Modify** option and follow the prompts.

Redirection

TARGET: Users of any type of file redirection (changing the default location of any of the folders used by the AWR Design Environment platform)

- In networked environments, some users may choose to change the default location for certain files.
- Complete information on redirection is available in the *AWR Design Environment Installation Guide* under "Configuring Program File Locations". If you use this capability, ensure that you make the same changes in AWR Design Environment platform V16 software that you set up for AWR Design Environment platform V15.