cadence®

Getting Started with Cadence Verification IP

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Contents

1

Preface

This manual describes the steps involved in getting started with a Cadence® Verification IP product. You will find useful information on various aspects of using a Cadence VIP product. This preface provides a general introduction to this manual and contains the following sections:

1.1 Documentation

Cadence Verification IP documentation is only available online. Click the following link or copy and past the URL in your browser.

https://support.cadence.com/apex/platformPage?searchTerm=Verification%20IP&pageName=VerificationIP

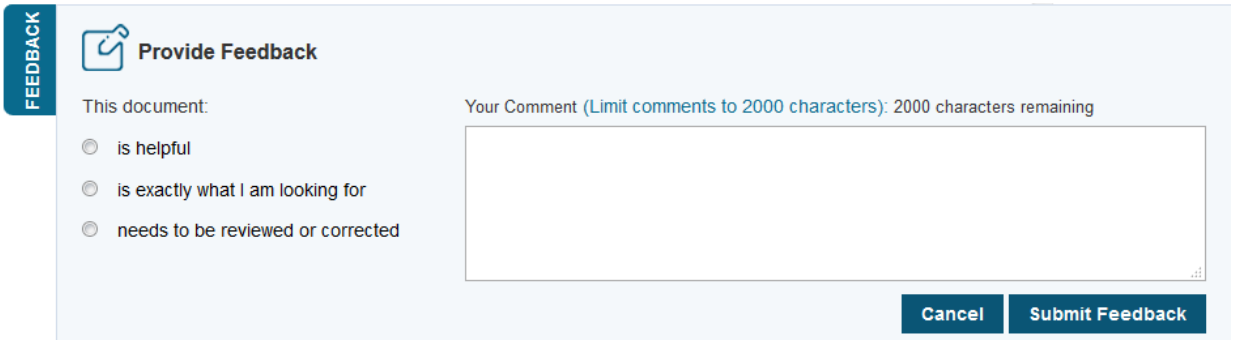
Use your Cadence username and password to access the above link. If you do not have one, click here to create one.

A short video shows how to access Cadence Verification IP documentation online.

For more information about Cadence Verification IP, read the following documents:

Document Name	Description
VIP Catalog Product Introduction	Contains an introduction to each product in the VIP Catalog.
Memory Model Portfolio Reference	Contains information common to all memory models.
Download UVM (Standard Universal Verification Methodology)	UVM (Universal Verification Methodology) documentation is available from Accellera.

Contact Cadence Customer Support to open a service request if you find an error, missing information, or difficulty accessing information. Use the feedback form in the online document or e-mail support@cadence.com.



1.2 Customer Support

The Cadence VIP Catalog is supported by Cadence Global Customer Support. Customers with a maintenance contract with Cadence can obtain current information on the tools at the following web site: http://support.cadence.com or e-mail support@cadence.com.

The Cadence Online Support provides access to advanced use training for selected protocols, expanded collateral such as Application Notes and Rapid Adoption Kits (RAKs), and product documentation.

2

Getting Started

This section provides you an introduction to various aspects of using Cadence Verification IP Catalog products, and links to more detailed information. The following topics are discussed:

- Licensing
- Download and Installation
- Running a Demo
- Setup Scripts
- Configuration and Integration
- Run-time Control
- Error Injection
- UVM API
- Popular Training Material

2.1 Licensing

VIP Catalog releases allow you access to UVC, ABVIP, PureSpec, and Memory Model technology. For more details, see VIP Licensing Guide.

License Type	Description
A La Carte License	Authorizes access to an individual VIP (for example, I2C) or feature (for example, TripleCheck) in a single simulation. This includes emerging protocols and emerging Memory Models.
VIP_Portfolio_Catalog License	Authorizes access to a single VIP in the VIP Portfolio in a single simulation. (For example, if a portfolio contains Ethernet and I2C, a checkout of this license would grant the use of either Ethernet or I2C, but not both.)
SoC Portfolio License	Authorizes access to all VIP products in the VIP Portfolio in a single simulation. (For example, if an SoC package contains Ethernet and I2C, a checkout of this license would grant the use of both Ethernet and I2C to the same simulation.)
Memory Model Portfolio License	Authorizes access to all Memory Models of the MM Portfolio in a single simulation.

2.2 Download and Installation

The installation process simplified for improved download time. For this purpose, starting VIPCAT 11.30.048 release the VIP Catalog is delivered in two `tar.gz` files without the use of InstallScape.

However, you must use InstallScape for versions earlier than VIPCAT 11.30.045.

For more details, see VIP Catalog Download and Installation.

2.3 Running a Demo

Running a demo helps you to confirm that the environment is set up properly to start using the VIP and learn its capabilities. After successfully running the demo, you can also set up a sandbox environment to further explore the VIP by integrating the VIP to your environment.

Detailed instructions for setting up your environment and running a demo is included in each "*<protocol> Reference for UVM SystemVerilog*" or "*<protocol> User Guide and Reference for UVM SystemVerilog*". See Verification IP Product Manuals.

2.4 Setup Scripts

The Cadence VIP installation includes several scripts to help you set up the VIP, check the VIP environment, and generate an example – all based on your specific environment characteristics (such as simulator, methodology, library location, and the like).

For more details on script syntax, options, and examples, see VIP Setup Scripts Reference.

Many examples are available in the VIP installation, which you can use as-is or modify to suit your needs. The following directories contain these examples, grouped by methodology:

- `$CDN_VIP_ROOT/tools/denali/example/<protocol>/svExamples/simpleExample`
- `$CDN_VIP_ROOT/tools/denali/ddvapi/sv/uvm/<protocol>/examples/simpleExample/` (for examples using SOMA configuration and UVM classes)
- `$CDN_VIP_ROOT/tools/denali/ddvapi/sv/uvm/<protocol>/examples/using_config_object/` (for examples using UVM Configuration objects)

The following video provides step-by-step instructions on VIP Scripting:

2.5 Configuration and Integration

You can use the UVM configuration flow for recommended VIPs with UVM, or SOMA flow for all VIPs. Step-by-step procedures for each flow is available.

For more information, see VIP Configuration and Integration Guide.

The following video provides step-by-step instructions on Integrating Cadence VIPs into your SystemVerilog UVM verification environment.

2.6 Run-time Control

The VIP model run-time control is managed using parameter settings contained in run-time control files. These files provide flexible ways to organize the settings. Several newly-available updates to the run-time control operations allow you to more precisely apply the settings. This document

provides an overview of the the enhancements as well as to the existing operations, as most existing operations continue to be available for backward compatibility.

For more information, see VIP Run-Time Control (.denalirc) Features Guide.

2.7 Error Injection

Error injection is a method for determining whether a design under test (DUT) conforms to the specification for the protocol. Transactions between the DUT and other components can be corrupt because of errors in timing or delays, or because of corrupted fields or signals. Injecting errors into a transaction in a controlled manner can help identify and correct defects in the DUT.

For more information, see VIP Error Injection Guide.

2.8 UVM API

The SystemVerilog UVM user API is made up of a set of SystemVerilog files. Each file contains one or more classes that describe the VIP model.

The VIPCAT release includes the following files:

- SystemVerilog base classes.
- UVM base classes that can be extended by the user.
- Example classes to run as a demo and use as a blueprint for your user classes.

For more information, see VIP UVM User API Guide.

2.9 Popular Training Material

Use the following links for available training material to gain knowledge on a specific Verification IP product.

- AMBA Verification IP (VIP) Training
- DisplayPort Verification IP (VIP) Training
- HDMI Verification IP (VIP) Training
- Ethernet Verification IP (VIP) Training
- MIPI Verification IP (VIP) Training
- PCIe Verification IP (VIP) Training

- USB Verification IP (VIP) Training

3

Advanced Topics

This section contains links to some of the popular advanced topics that are available in support.cadence.com on using Cadence Verification IP.
The support portal is updated regularly with newer topics.

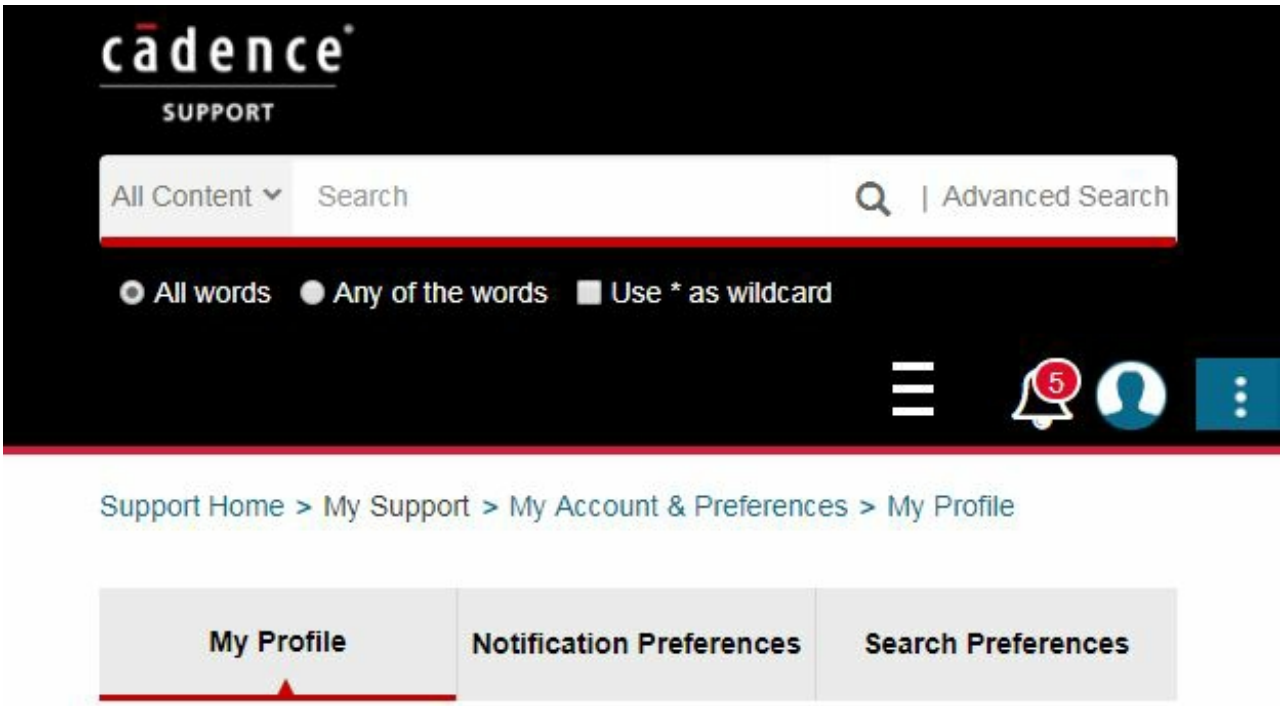
- Troubleshooting, Application Notes, and Error Messages
- Dynamic Activation
- Coverage
- Data-Driven Verification

3.1 Troubleshooting, Application Notes, and Error Messages

Cadence technical team has created a vast amount of knowledge base for the benefit of advanced users of Cadence Verification IP products. This pool of information is regularly updated.

- See Troubleshooting Information for Verification IP.
  There are more than 1500 troubleshooting articles available.
- See Application Notes for Verification IP.
  Dozens of application notes provide targeted solutions and explain complex verification scenarios.
- See Error Messages for Verification IP.
  Some error messages need more details and troubleshooting steps. You will find hundreds of such complex errors explained with examples where necessary.

In the Cadence support site, set **Notification Preferences** appropriately to receive alerts when there is new information or Cadence software.



3.2 Dynamic Activation

Dynamic activation is a selective instantiation feature that can provide significant savings in performance and capacity when you want to use just a subset of your VIP instances in a given simulation. Dynamic activation is similar to the traditional Cadence VIP instantiation flow, so it can typically be adopted with just a few changes.

For more information, see VIP Dynamic Activation Guide.

3.3 Coverage

Coverage is a measure of what percentage of functional DUT features were exercised. Cadence VIPs provide data-oriented functional coverage, which tracks data values and attributes of transactions to help you identify untested features of the protocol. Coverage is calculated and reported by the monitor part of the agent, and appears in the Incisive Metrics Center (IMC).

For more information, see VIP Coverage Guide.

3.4 Data-Driven Verification

The Data-Driven Verification API (DDVAPI) is an extension to the simulation environment offered

by MMAVTM and PureSpecTM for Verification IP software. The DDVAPI can be used to integrate applications within the simulation process.

The DDVAPI enables you to build custom applications for verification, such as self-checking test benches. Custom applications written with the DDVAPI can access and set memory content, and can register to be called when data activity (reads or writes) occur in the Memory Models.

For more information, see Data-Driven Verification API Reference.