APPCELL DEMO LIBRARY

ADD-ON TO CDNLIVE 2019 EMEA CUS-TECHTORIAL V

2019/05/23

VERSION 1

OVERVIEW

- appCell demo library
- Package files and folders
- Examples
- appCell development
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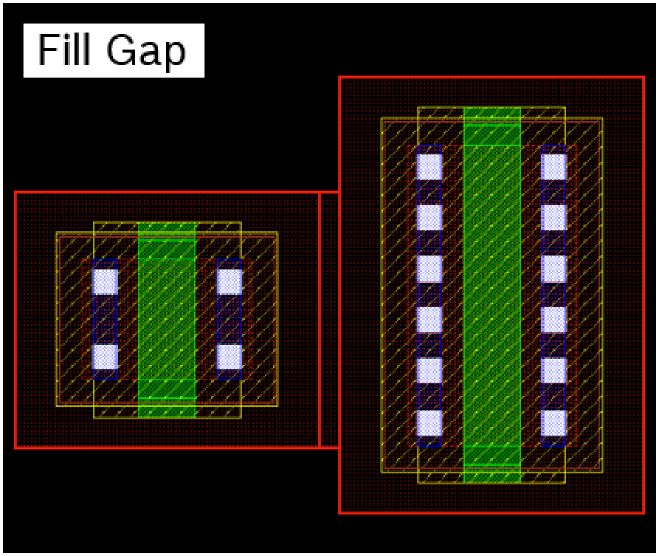
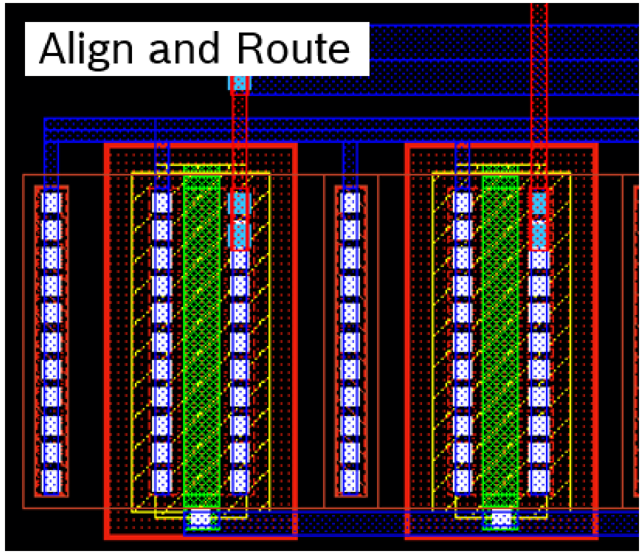
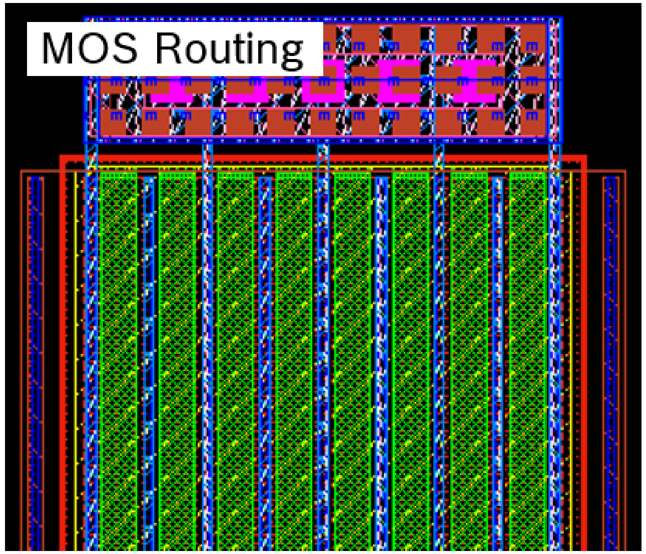
APPCELL DEMO LIBRARY

- appCells are PCells that act as "apps" within Virtuoso. They complement and enhance existing Virtuoso Schematic and Virtuoso Layout functionality, and they help designers to automate their daily work.
- appCells are provided to projects via libraries. Contrary to PCells, they do not create any dependencies in the final design.
- The appCell concept was first published and demonstrated at CDNLive EMEA 2019, Munich, 8 May 2019:
  (G. Jerke et al.: CUS-Techtorial V, "Custom silicon design automation with Cadence PCell Designer")
- This demo library contains several examples that can be used for demonstration, education and inspiration.


Fill Gap


Align and Route


MOS Routing

PACKAGE FILES AND FOLDERS

- appCellDemoLib/ → Deployed appCells ready to be used (PCell Designer tool is not needed)
- appCellDemoLib_Examples/ → Cells with example layouts (PCell Designer tool is not needed)
- appCellDemoLib_Toolbar.il → Adds toolbar to Virtuoso Layout (PCell Designer tool is not needed)
  This SKILL file also demonstrates the invocation of appCells within Virtuoso.

- appCellDemoLib_Dlvp/ → appCells development library (PCell Designer tool and license is needed)
- appCellDemoLib_Sources/ → appCells source code as text files to recreate the appCells in PCell Designer

Note: Unpack the tar.gz file with

```
tar xzf appCellDemoLib_20190523.tar.gz
```

Requires Cadence GPDK gpdk045.
PCell Designer tool is not needed.

EXAMPLES

(Deployed) appCell examples in *appCellDemoLib* library:

advancedAlignAppCell → Align and route a selected set of MOS transistor instances

fillGapsAppCell → Fill the gap between MOS transistor instances

routeMosAppCell → Create the multi-layer route metallization of MOS transistor instances

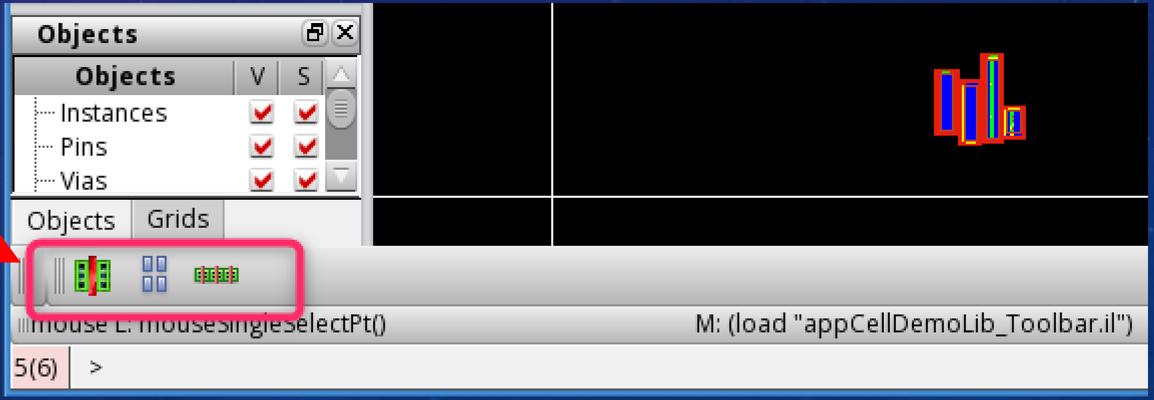
Requires Cadence GPDK gpdk045.
PCell Designer tool is not needed.

EXAMPLES (2)

Execute the following steps to run the appCell demos:

1. Add the libraries *appCellDemoLib* and *appCellDemoLib_Examples* to your cds.lib file
2. Start Virtuoso Layout (IC617, IC618, IC12.3, IC18.1)
3. Open one of the appCell example layouts from the *appCellDemoLib_Examples* library
4. Load the appCell demo toolbar in the CIW:

```
(load "appCellDemoLib_Toolbar.il")
```

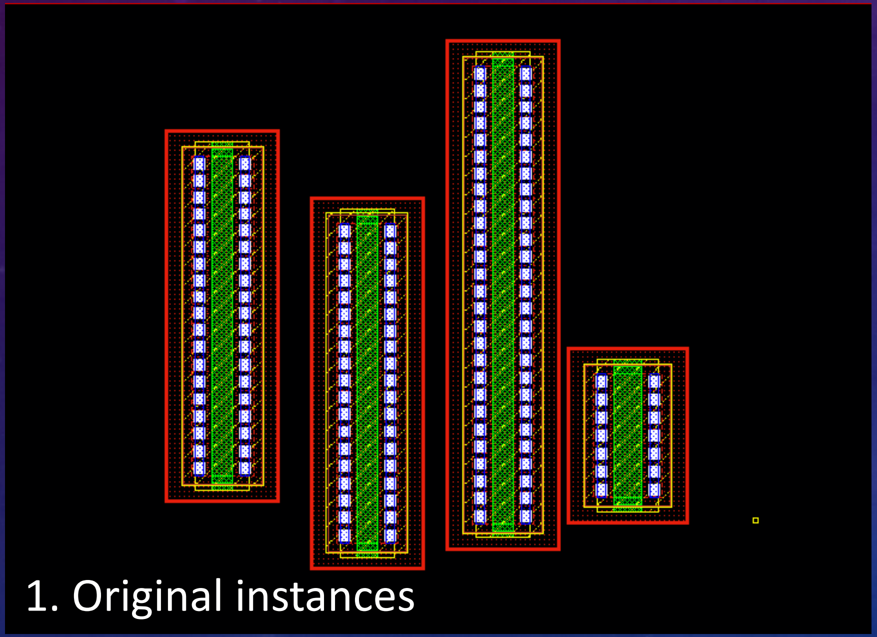


```
mouse L: mouseSingleSelectPt()        M: (load "appCellDemoLib_Toolbar.il")
5(6)  >
```

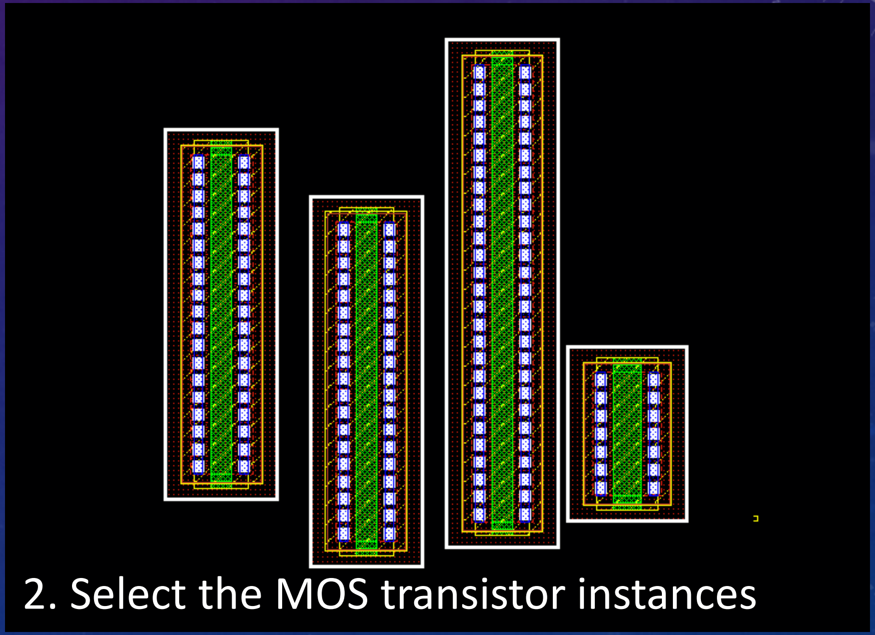
Requires Cadence GPDK gpdk045.
PCell Designer tool is not needed.

EXAMPLES (3)

5. Execute the appCells based on the layout example:



1. Original instances



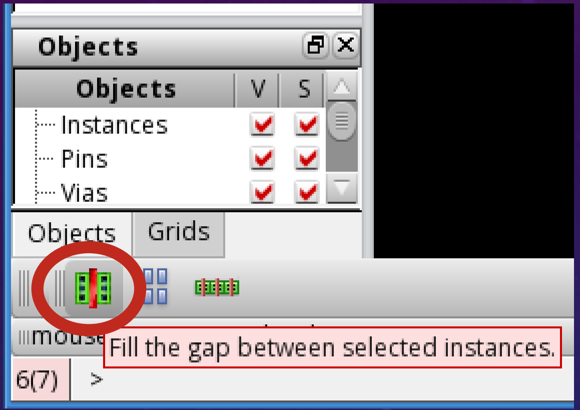
2. Select the MOS transistor instances

Example: appCellDemoLib_Examples / demo_fillGapsAppCells

Requires Cadence GPDK gpdk045.
PCell Designer tool is not needed.

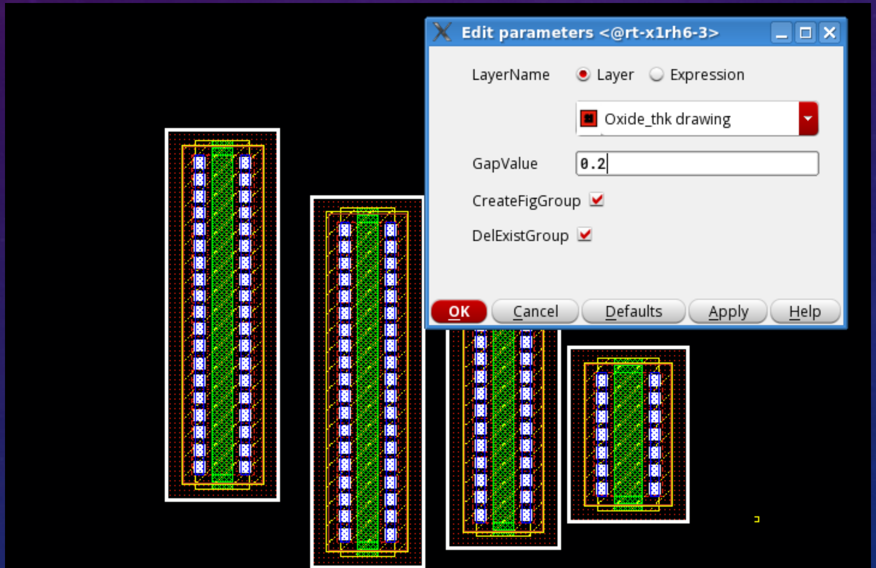
EXAMPLES (4)

5. Execute the appCells based on the layout example:



Fill the gap between selected instances.

3. Invoke the FillGap appCell from the appCell toolbar



LayerName ● Layer ○ Expression

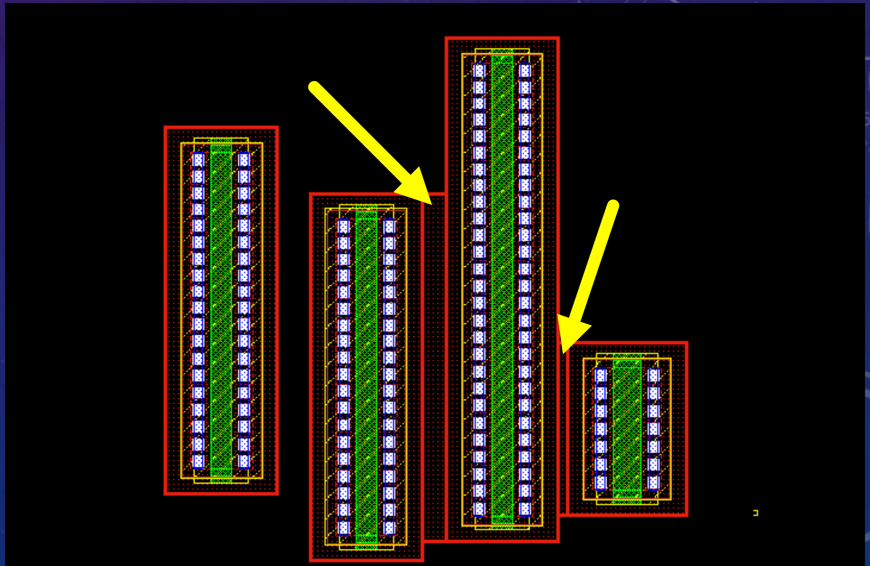
🟥 Oxide_thk drawing

GapValue 0.2

CreateFigGroup ☑

DelExistGroup ☑

4. Choose the appCell parameters



5. Created filler polygons for all gaps ≤ 0.2

Please note that the appCell does not leave any traces in the layout.

Example: appCellDemoLib_Examples / demo_fillGapsAppCells

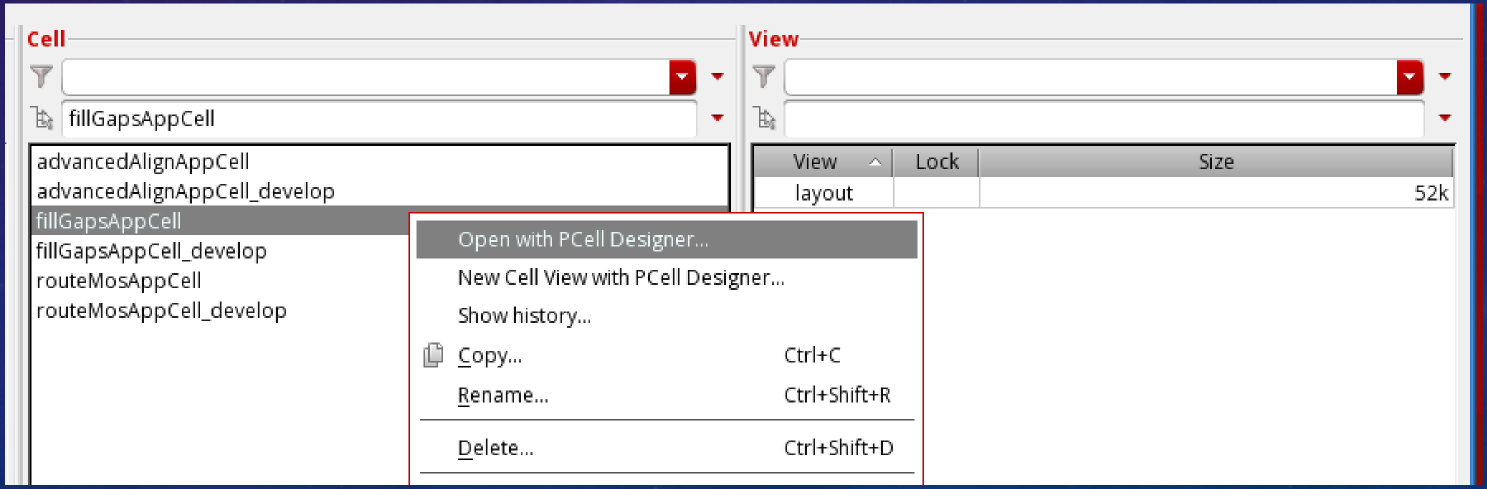
Requires Cadence GPDK gpdk045.
PCell Designer tool is needed.

APPCELL DEVELOPMENT

1. Add the library *appCellDemoLib_Dlvp* to your cds.lib file
2. Start Virtuoso Layout (IC617, IC618, IC12.3, IC18.1)
3. In CIW load Cadence PCell Designer version 2.5.9 or newer (can also be done via .cdsinit):

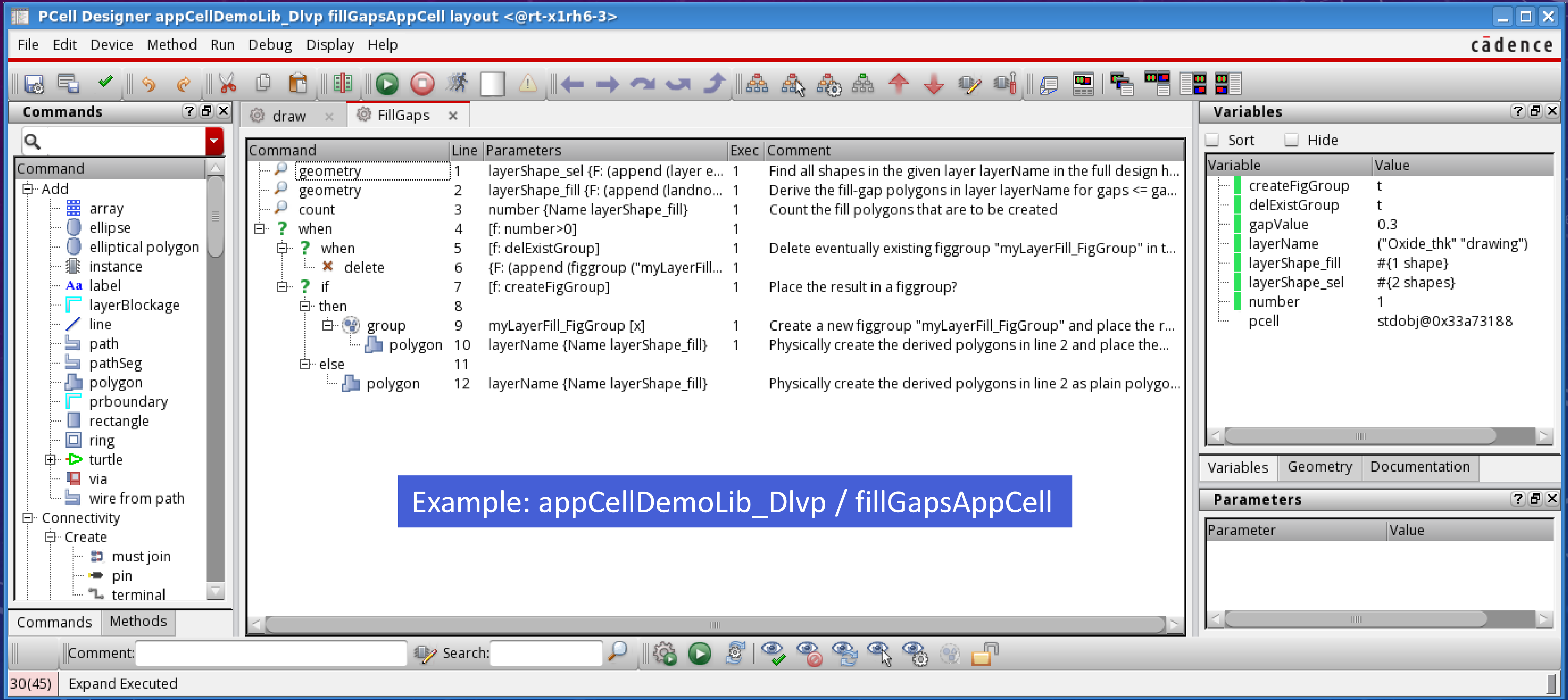
```
(loadContext "PCellDesigner-2-5-9.cxt")
```

4. In Library Manager navigate to library *appCellDemoLib_Dlvp* and open an appCell with PCell Designer:



Requires Cadence GPDK gpdk045.
PCell Designer tool is needed.

APPCELL DEVELOPMENT (2)



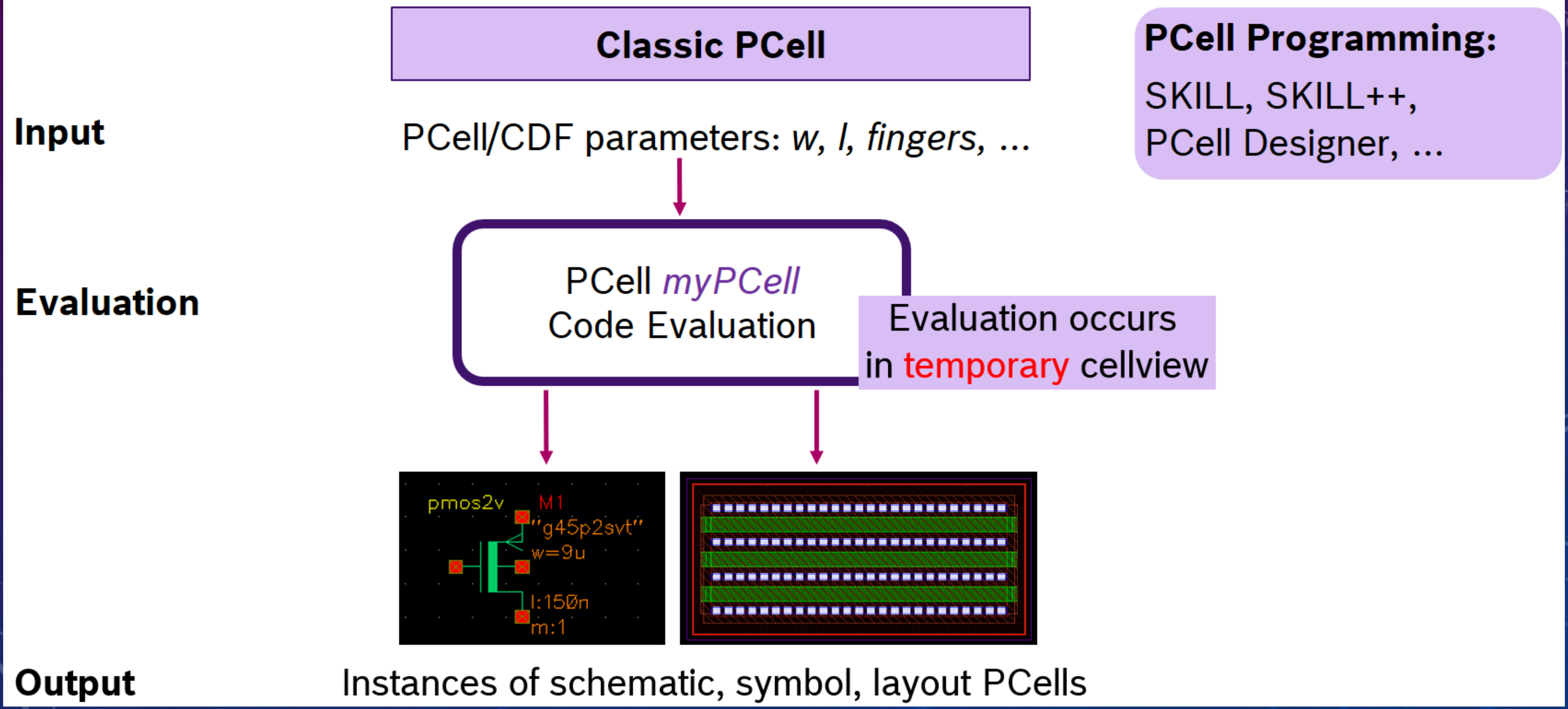
Command	Line	Parameters	Exec	Comment
geometry	1	layerShape_sel {F: (append (layer e...	1	Find all shapes in the given layer layerName in the full design h...
geometry	2	layerShape_fill {F: (append (landno...	1	Derive the fill-gap polygons in layer layerName for gaps <= ga...
count	3	number {Name layerShape_fill}	1	Count the fill polygons that are to be created
when	4	[f: number>0]	1	
when	5	[f: delExistGroup]	1	Delete eventually existing figgroup "myLayerFill_FigGroup" in t...
delete	6	{F: (append (figgroup ("myLayerFill...	1	
if	7	[f: createFigGroup]	1	Place the result in a figgroup?
then	8			
group	9	myLayerFill_FigGroup [x]	1	Create a new figgroup "myLayerFill_FigGroup" and place the r...
polygon	10	layerName {Name layerShape_fill}	1	Physically create the derived polygons in line 2 and place the...
else	11			
polygon	12	layerName {Name layerShape_fill}		Physically create the derived polygons in line 2 as plain polygo...

Variable	Value
createFigGroup	t
delExistGroup	t
gapValue	0.3
layerName	("Oxide_thk" "drawing")
layerShape_fill	#{1 shape}
layerShape_sel	#{2 shapes}
number	1
pcell	stdobj@0x33a73188

30(45) Expand Executed

Example: appCellDemoLib_Dlvp / fillGapsAppCell

APPCELLS VS. CLASSIC PCELLS



Classic PCell

PCell Programming:

SKILL, SKILL++,
PCell Designer, …

Input

PCell/CDF parameters: *w*, *l*, *fingers*, …

Evaluation

PCell *myPCell*
Code Evaluation

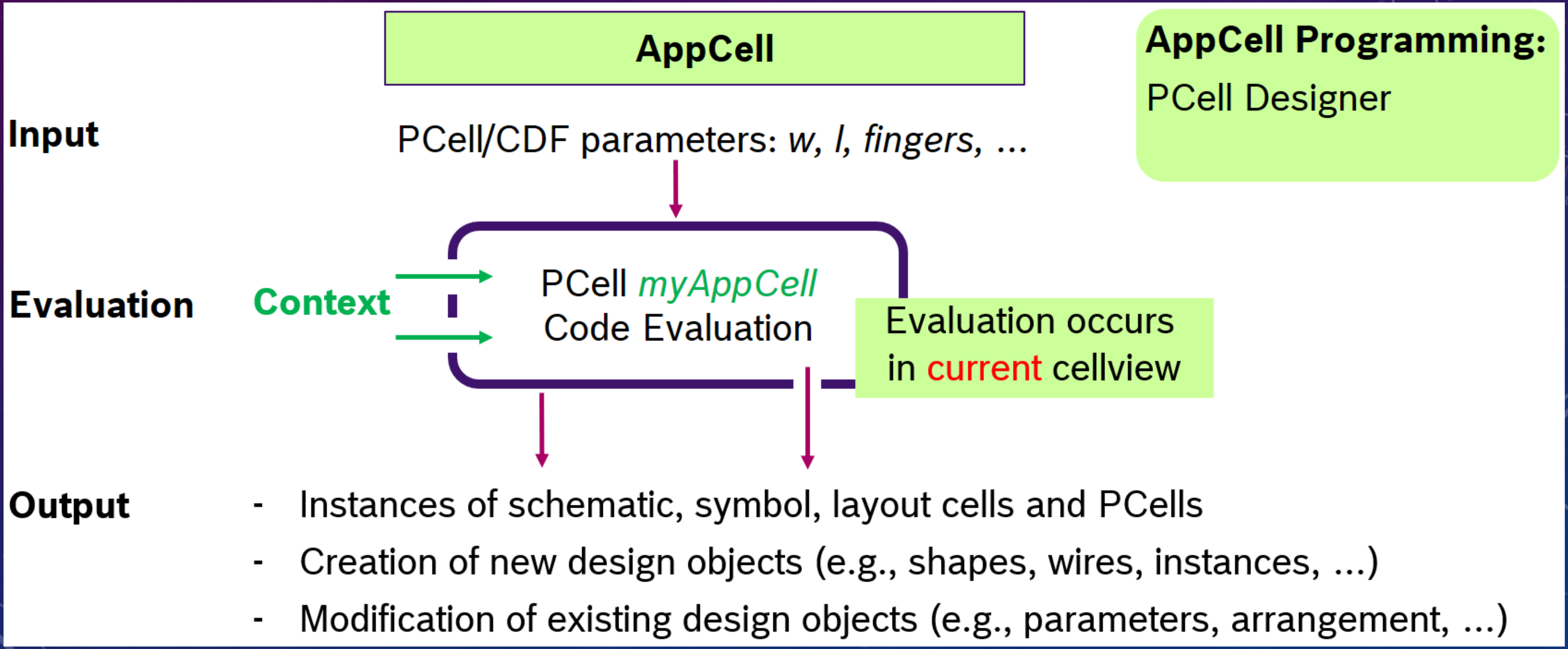
Evaluation occurs
in temporary cellview

Output

Instances of schematic, symbol, layout PCells

Source: CDNLive EMEA 2019, CUS-Techtorial V

APPCELLS VS. CLASSIC PCELLS (2)



AppCell

AppCell Programming:

PCell Designer

Input

PCell/CDF parameters: *w*, *l*, *fingers*, …

Evaluation

Context

PCell *myAppCell*
Code Evaluation

Evaluation occurs in current cellview

Output

- Instances of schematic, symbol, layout cells and PCells
- Creation of new design objects (e.g., shapes, wires, instances, …)
- Modification of existing design objects (e.g., parameters, arrangement, …)

Source: CDNLive EMEA 2019, CUS-Techtorial V

DISCLAIMER

The appCell demo library is provided "as is" and purely intended for demonstration, education and inspiration.

Use it freely, but use it at your own risk!

CONTRIBUTORS

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Please consider to share your thoughts and examples as well in the PCell Designer Community Forum. We hope you find the provided appCellDemoLib examples helpful and inspiring ☺.

https://community.cadence.com/cadence_technology_forums/f/pcell-designer