By development of this model we have tried to solve the following aspects:

- the real topology of circuit;
- the real voltage level of circuit pins;
- the variation with VCO free-running frequency of PLL parameters: oscillator sensitivity, the lock bandwidth;
- the variation with supply voltage of following parameters: oscillator sensitivity and lock bandwidth.

The structural architecture with connection diagram is shown in figure 2. It can see that the VCO free-running frequency is determinated by external components C_0 and R_0. Also, the low-pass loop filter must be connected to the integrated circuit. In concordance with manufacturer indications, a simple lag filter or a lag-lead filter may by used. These kind of filters are forming from internal resistance at pin 7 (with value $3{,}6K\Omega$) and suitable external components.

According with the data sheet, the circuit performances in close loop are given by the following relationships:

$$f_0 = \frac{0.27}{R_0 \cdot C_0} \tag{10}$$

$$K_0 = \frac{54 \cdot f_0}{V_{a\lim}} \tag{11}$$

$$K_D = 0{,}68\ V/rad \tag{12}$$

$$B_U = \frac{16 \cdot f_0}{V_{a\lim}} \tag{13}$$

$$B_C = 2 \cdot \sqrt{2} \cdot f_n$$

$$f_n = \frac{1}{2 \cdot \pi} \cdot \sqrt{\frac{K_0 \cdot K_D}{\tau_1}} \quad \text{for simple lag filter} \tag{14}$$

$$f_n = \frac{1}{2 \cdot \pi} \cdot \sqrt{\frac{K_0 \cdot K_D}{\tau_1 + \tau_2}} \quad \text{for lag - leag filter}$$

$$V_{REF} = \frac{12{,}15K\Omega \cdot V_{\text{alim}}^{+} + 1{,}75K\Omega \cdot \left(V_{\text{alim}}^{-} + V_{BE}\right)}{13{,}85K\Omega} = \tag{15}$$
$$= 0.126354 \cdot \left(V_{\text{alim}}^{-} + V_{BE}\right) + 0{,}877256 \cdot V_{\text{alim}}^{+}$$

In figure 3 is shown the developed behavioral model of the PLL integrated circuit LM565. It is shown also the created SPICE symbol. The functional terminals of symbol correspond with the pins of LM565 package. The SPICE netlist of developed model is:

```
.SUBCKT LM565-X 1 2 3 4 5 6 7 8 9 10
C_C1 0 init 1u
R_R3 $N_0001 6  1.75k
R_R4 0 init 1g
R_R6 8 9 10g
R_R2 3 0 10g
R_R1 $N_0002 7 3.6k
E_E15 $N_0002 0 VALUE { V($N_0003, 0)+V(6,0) }
E_E1 $N_0003 0 TABLE { 0.68*V(2, 0)*V(5,0) }
+ ( (-0.68,-0.68) (0.68,0.68) )
G_G1 init 0 VALUE { (V(7,
+ 0)-V(6,0))*0.00001458/(R0*C0*(V(10,0)-V(1,0))) }
E_E13 4 0 VALUE
{sin(6.28*(0.27/(R0*C0))*(time+(R0*C0/(6.28*0.27))
*V(0,init))) }
```

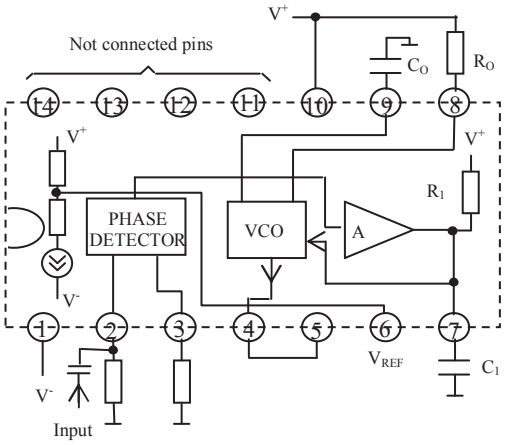

Figure 2. The structural architecture with connection diagram of LM565

```
E_E3 $N_0001 0 VALUE
{0.126354*(0.7+V(1,0))+0.873646*V(10,0) }
.ENDS
```

A transient analysis is run to analyze the capture and lock ranges. The PLL input is attacked by a signal those frequency firstly rises from a lower value (lower than $f_0 - B_C/2$) at a value greater than $f_0 + B_U/2$, and secondly diminishes from a value greater than $f_0 + B_C/2$ to a value lower than $f_0 - B_U/2$. The schema used for simulation with the simulation results is shown in figure 4. It can see that the PLL does not respond to the input signal until the input signal frequency reaches the lower capture range frequency. Once lock is attained, the output voltage of PLL tracks frequency changes of the input signal and orders changes to the VCO frequency. But, when the input frequency exceeds the upper lock range frequency the PLL output voltage suddenly drops. Similarly, at the diminishing of frequency the PLL output does not respond until the input signal frequency reaches the upper capture range frequency and, once lock is attained, the PLL output voltage changes VCO frequency. When the lower lock range reaches, the PLL output voltage also suddenly drops. It can see also that for the chosen VCO free-running frequency and supply voltage, the values of capture and lock ranges respect the relations (13) and (14). The simulation time of these analyses, for a step ceiling of 25us and a print step of 25us, was around 8s.

We use this behavioral model of LM656 integrated circuit to simulate some typical applications given in his data sheet. Firstly, we simulate the FM demodulator application. The schema used for simulation and the simulation result are presented in figure 5. The simulation time, for a step ceiling of 2.5us and a print step of 2.5us, was around 4s. Next, we simulated a FSK demodulator, presented with the simulation result and input stimulus in figure 6. For this application, the simulation time, for a step ceiling of 25us and a print step of 25us, was around 15s. The last simulated application was a frequency multiplier.