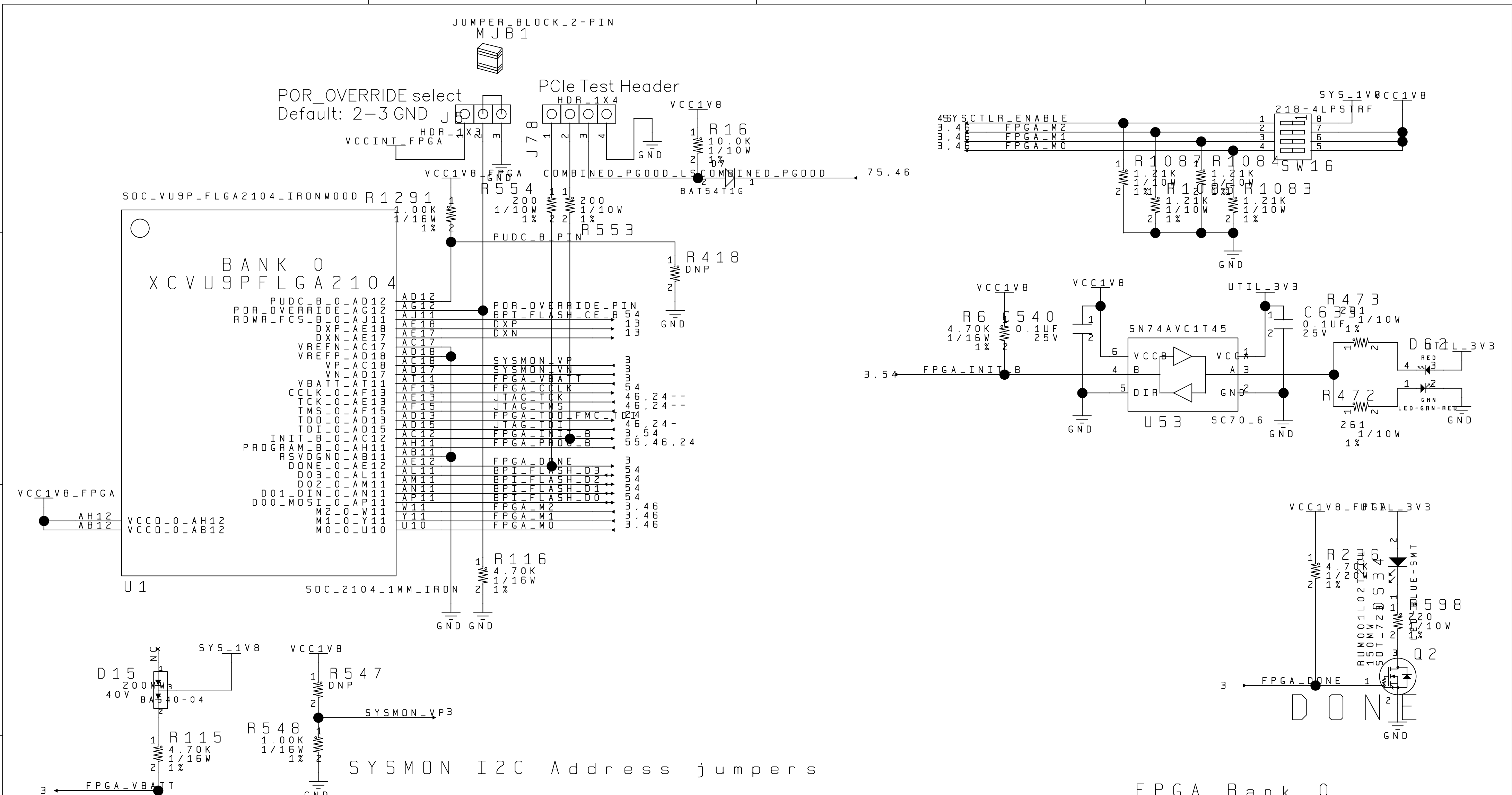
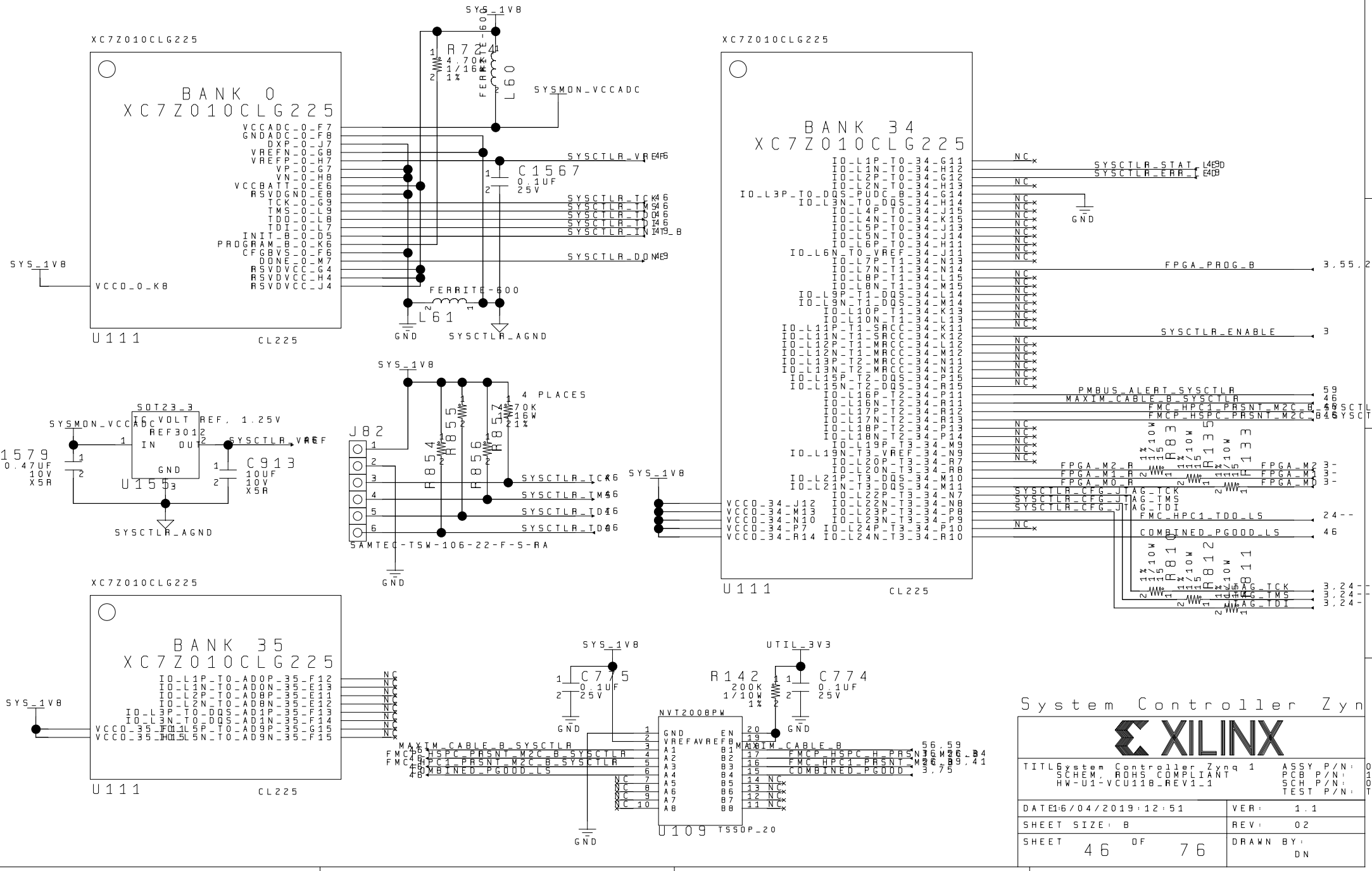


FPGA Bank 0

XILINX

TITLE FPGA Bank 0 SCHEM, ROHS COMPLIANT HW-U1-VCU118_REV1_1	ASSY P/N: PCB P/N: SCH P/N: TEST P/N:
DATE 16/04/2019 12:50	VER: 1.1
SHEET SIZE: B	REV: 02
SHEET 3 OF 76	DRAWN BY: DN


XC7Z010CLG225
BANK 0
XC7Z010CLG225
VCCADC_O_F7
GNDADC_O_F8
DXP_O_J7
VREFN_O_G8
VREFP_O_H7
VP_O_G7
VN_O_H8
VCCBATT_O_E6
RSVDGND_E8
TCK_O_G9
TMS_O_L9
TDO_O_L8
TDI_O_L7
INIT_B_O_D5
PROGRAM_B_O_K6
CFGBVS_O_F6
DONE_O_M7
RSVDVCC_G4
RSVDVCC_H4
RSVDVCC_J4
VCCO_0_K8
SYS_1V8
U111
CL225
R724
4.70K
1/16W
1%
FERRITE-600
L60
SYSMON_VCCADC
C1567
0.1UF
25V
SYSCTLR_VREF
SYSCTLR_TCK
SYSCTLR_TMS
SYSCTLR_TDO
SYSCTLR_TDI
SYSCTLR_INIT_B
SYSCTLR_DONE
FERRITE-600
L61
GND
SYSCTLR_AGND
SOT23_3
10 VOLT REF, 1.25V
REF3012
IN
OUT
GND
U155
C1579
0.47UF
10V
X5R
C913
10UF
10V
X5R
J82
4 PLACES
R854
R855
R856
R857
470K
1/16W
1%
SAMTEC-TSW-106-22-F-S-RA
XC7Z010CLG225
BANK 34
XC7Z010CLG225
IO_L1P_T0_34_G11
IO_L1N_T0_34_H12
IO_L2P_T0_34_G12
IO_L2N_T0_34_H13
IO_L3P_T0_DQS_PUDC_B_34_G14
IO_L3N_T0_DQS_34_H14
IO_L4P_T0_34_J15
IO_L4N_T0_34_K15
IO_L5P_T0_34_J13
IO_L5N_T0_34_J14
IO_L6P_T0_34_H11
IO_L6N_T0_VREF_34_J11
IO_L7P_T1_34_N13
IO_L7N_T1_34_N14
IO_L8P_T1_34_L15
IO_L8N_T1_34_M15
IO_L9P_T1_DQS_34_L14
IO_L9N_T1_DQS_34_M14
IO_L10P_T1_34_K13
IO_L10N_T1_34_L13
IO_L11P_T1_SRCC_34_K11
IO_L11N_T1_SRCC_34_K12
IO_L12P_T1_MRCC_34_L12
IO_L12N_T1_MRCC_34_M12
IO_L13P_T2_MRCC_34_N11
IO_L13N_T2_MRCC_34_N12
IO_L15P_T2_DQS_34_P15
IO_L15N_T2_DQS_34_R15
IO_L16P_T2_34_P11
IO_L16N_T2_34_R11
IO_L17P_T2_34_R12
IO_L17N_T2_34_R13
IO_L18P_T2_34_P13
IO_L18N_T2_34_P14
IO_L19P_T3_34_M9
IO_L19N_T3_VREF_34_N9
IO_L20P_T3_34_R7
IO_L20N_T3_34_R8
IO_L21P_T3_DQS_34_M10
IO_L21N_T3_DQS_34_M11
IO_L22P_T3_34_N7
IO_L22N_T3_34_N8
IO_L23P_T3_34_P8
IO_L23N_T3_34_P9
IO_L24P_T3_34_P10
IO_L24N_T3_34_R10
VCCO_34_J12
VCCO_34_M13
VCCO_34_N10
VCCO_34_P7
VCCO_34_R14
SYS_1V8
U111
CL225
NC
SYSCTLR_STAT_LED
SYSCTLR_ERR_LED
GND
FPGA_PROG_B
SYSCTLR_ENABLE
PMBUS_ALERT_SYSCTLR
MAXIM_CABLE_B_SYSCTLR
FMC_HPC1_PRSNT_M2C_B_SYSCTLR
FMCP_HSPC_PRSNT_M2C_B_SYSCTLR
FPGA_M2_R
FPGA_M1_R
FPGA_M0_R
SYSCTLR_CFG_JTAG_TCK
SYSCTLR_CFG_JTAG_TMS
SYSCTLR_CFG_JTAG_TDI
FMC_HPC1_TDO_LS
COMBINED_PGOOD_LS
R833
R835
R837
R810
R812
R811
XC7Z010CLG225
BANK 35
XC7Z010CLG225
IO_L1P_T0_AD0P_35_F12
IO_L1N_T0_AD0N_35_E13
IO_L2P_T0_AD8P_35_E11
IO_L2N_T0_AD8N_35_E12
IO_L3P_T0_DQS_AD1P_35_F13
IO_L3N_T0_DQS_AD1N_35_F14
IO_L15P_T2_DQS_AD9P_35_G15
IO_L15N_T2_DQS_AD9N_35_F15
VCCO_35_F11
VCCO_35_H15
SYS_1V8
U111
CL225
C775
0.1UF
25V
R142
200K
1/10W
1%
UTIL_3V3
C774
0.1UF
25V
NVT2008PW
U109
TSSOP_20
GND
VREFA
VREFB
A1
A2
A3
A4
A5
A6
A7
A8
B1
B2
B3
B4
B5
B6
B7
B8
MAXIM_CABLE_B_SYSCTLR
FMCP_HSPC_PRSNT_M2C_B_SYSCTLR
FMC_HPC1_PRSNT_M2C_B_SYSCTLR
COMBINED_PGOOD_LS
MAXIM_CABLE_B
FMCP_HSPC_H_PRSNT
FMC_HPC1_PRSNT_M2C_B
COMBINED_PGOOD
System Controller Zynq
XILINX
TITLE: System Controller Zynq 1
SCHEM, ROHS COMPLIANT
HW-U1-VCU118_REV1_1
ASSY P/N:
PCB P/N:
SCH P/N:
TEST P/N:
DATE: 6/04/2019 12:51
VER: 1.1
SHEET SIZE: B
REV: 02
SHEET 46 OF 76
DRAWN BY: DN