BTC Footprint Guidelines

1. ePad (thermally enhanced)
    a. Metal Layer
        i. Equal to nominal exposed pad of package from Data Sheet POD
        ii. Thermal vias diameter should be 0.3 to 0.33mm
        iii. Typical center to center distance of vias is 0.86mm (33mil) with a 0.55mm (22mil) clearance between drill holes.
            1. Clearance may vary depending on ePad size
        iv. Number of thermal vias are based on the thermal dissipation requirements and ePad size.
        v. Typically, LCLD recommends open type via type with wall plating
            1. The via type may change dependent on PCB surface finishes used and ePad size.
            2. See IPC 7093B section 6.11 for thermal pad design options
            3. See IPC 7093B Table 6-2 BTC Thermal Pad Design Option Pros and Cons, this provides factors to consider for via type decisions
    b. SM Layer - NSMD (Non Solder Mask Defined)
        i. Solder mask opening is typically larger than the copper pad by 0.0502mm (2 mil) but not less than 0.0254mm (1 mil)
            1. IPC7093B section 6.4 recommends SMD, however through experimentation and measurement we have found that NSMD allows for better self-alignment and resulting package planarity during package draw down during the liquidous reflow stage.
    c. PM layer – used for the PM Stencil. These rules below reduce voiding, provide good solder coverage and target standoff of 0.063mm (63um) – IPC7093 section 6.13.1
        i. Window paned with aligning streets with vias as much as practical
        ii. Minimum paste to pad ration of 50% and maximum of 80%
        iii. Street width minimum 0.3mm (target is the diameter of via used)
        iv. All stencil openings must have a minimum corner radius of 0.0502mm (50um)

2. IO Pins
    a. Metal
        i. PCB metal should be equal to nominal exposed pin of package from POD (preferred) or data sheet, and also match the shape of the package pin
        ii. Outside of package area extend the pad by a minimum of 0.2mm (~8mil).
    b. SM
        i. IO Pins must be NSMD
            1. This allows for solder to flow along the side walls of the PCB metal
        ii. NSMD SM opening is typically larger than the copper pad by 0.025mm (~1 mil)
        iii. Pin to pin SM clearance should be a minimum of 0.2mm, and in some cases larger depending on PCB fabricator DFM rules
        iv. NSMD is desired with a minimum 0.0502mm (2mil) pull-back from the Copper if possible
            1. IPC 7093B section 6.4
    c. PM (non-wettable flank design)
        i. Must use a 0.127mm (5mil) stencil for a target standoff of 0.0635mm (2.5mil) after reflow
        ii. All stencil openings must have a minimum corner radius of 0.05mm (50um) (See section 1.c)
        iii. Pin PM extends beyond the edge of the package by the radius of the oblong

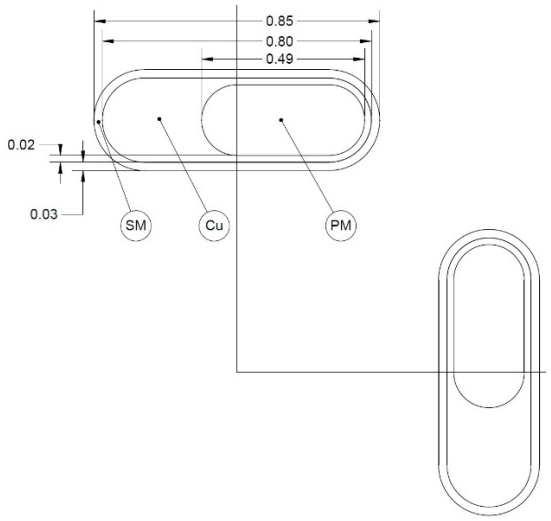


Figure 1 Example of a Non wettable Flank IO Pin Design

        iv. Dimension of the stencil openings under the package should be 20 to 30 µm smaller than the size of the corresponding copper lands.

Examples of poor and good solder attachment on a large QFN device

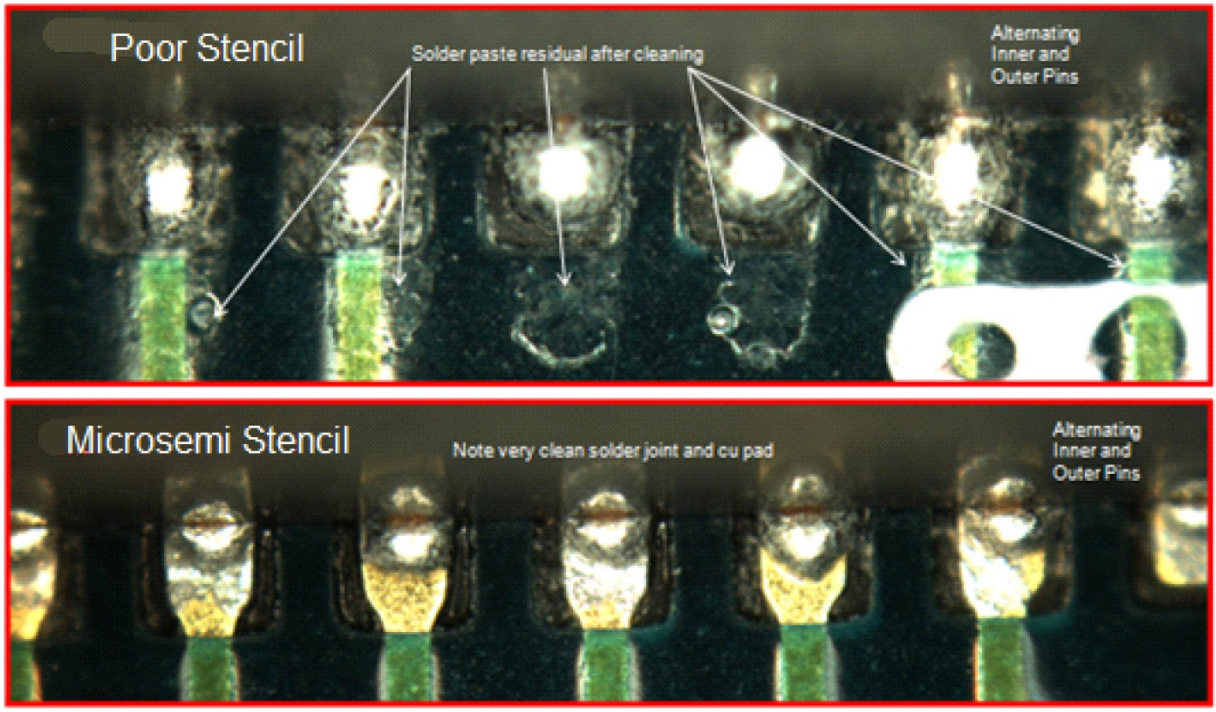


Figure 2IO Pin Solder Joint (non-Wettable Flank)

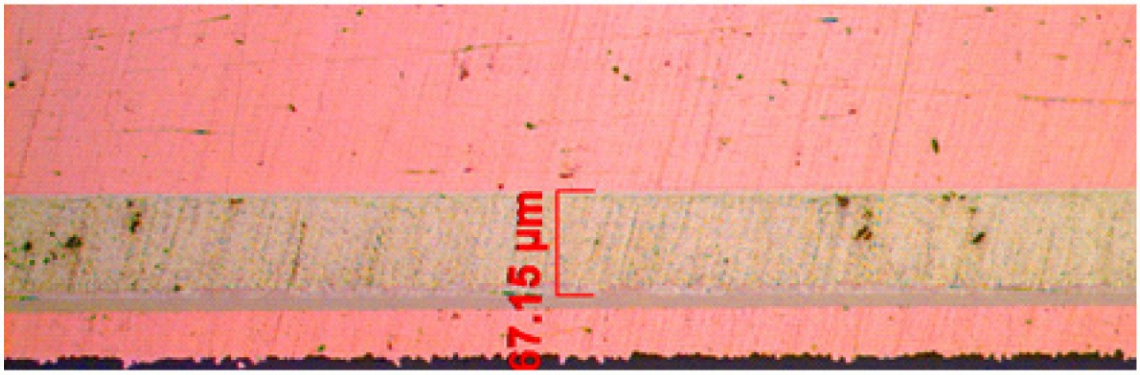
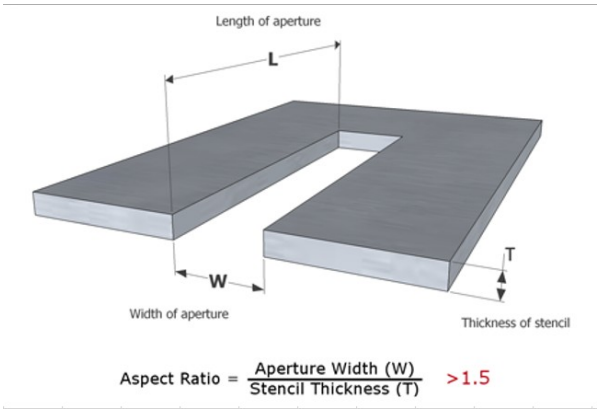
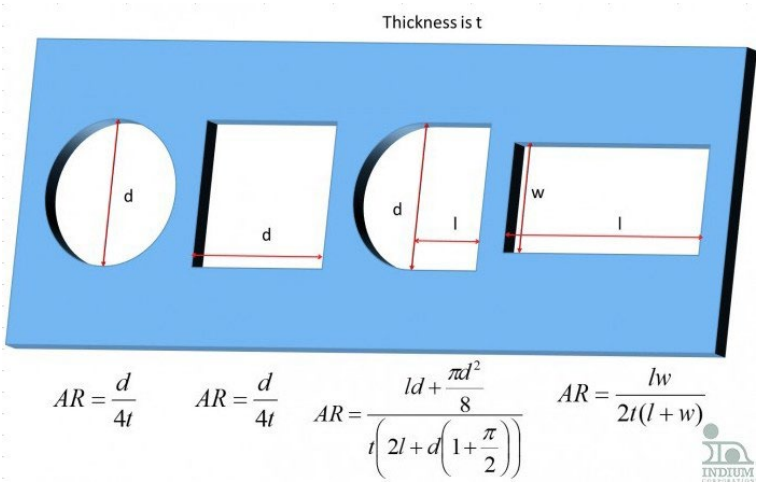


Figure 3QFN ePad Standoff height = 67.1 um

3. Stencil design for solder paste application (IPC7093A Recommendation - Section 7.5.1)
    a. Use a 127um (5mil) stencil thickness to achieve a final standoff of 63.5um (2.5mil) after reflow
        i. Note: IPC7093 Stencil thickness recommendation range is from 76um to 152um this provides a final standoff of 50um to 75um after reflow (section 7.5.1)
    b. Aspect Ratio
        i. The aspect ratio of over 1.5 prevents ensures proper paste release



    c. Area Ration
        i. The area ratio of over 0.66 prevents ensures proper paste release



    d. Corner radius
        i. The stencil openings corner radius must be larger than the solder power diameter to avoid solder release defects. i.e. Type 3 maximum particle size is 50um, the recommendation is to use a corner radius greater than 0.05mm (50um)
        ii. The corner radius prevents solder power from contacting 2 walls of the stencil which could create stencil release defects.

4. Acronyms/Definitions
    a. BTC – Bottom Terminated Components
    b. PCB – Printed Circuit Board
    c. SM – Solder mask also known as solder resist
    d. PM – Paste Mask, this is a stencil use in the application of solder paste to the PCB before device mounting
    e. ePad – Exposed metal pad/s on the bottom of device package, not the IO Pins
    f. SMD – Solder Mask Defined
        i. Opening in the PCB solder mask exposing the metal layers with the area of the exposed metal is defined by the Solder Mask. Metal is larger than solder mask opening.
    g. NSMD - Non Solder Mask Defined
        i. Opening in the PCB solder mask exposing the metal layers with the area of the exposed metal is defined by the metal layer. Metal is smaller than the solder mask opening.

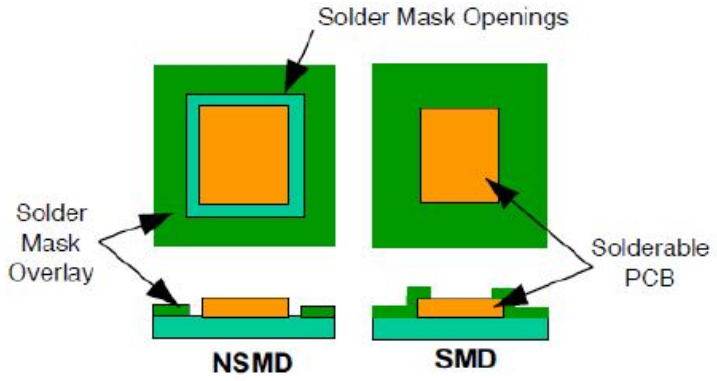


Figure 4- Image taken from Digikey Tech Forum

    h. POD – Package Outline Drawing. The POD includes mechanical dimensions with tolerances of the device package.
    i. Standoff – Distance from the ePad and IO Pins features to the PCB metal attachment, it is often referred to Bond Line thickness. The mounted device reliability (IPC7902 testing) is directly related to the standoff height of the solder attachment. The standoff height target for acceptable life expectancy is 63um, range is 50um to 76um.
    j. DFM – Design For Manufacturablity

5. References
    a. IPC 7093B release date October 2020
    b. Microsemi Document ID# 148192 title: Dual Row QFN Stencil DesignLe792388VQC Product December 2013 – Available upon request
    c. NXP document AN1902 rev.9 April 2021 - Assembly guidelines for QFN (quad flat no-lead) and SON (small outline no-lead) packages