Cadence Stackup Setting for Signal Integrity

Ron Dallas, Teradyne Inc.

Abstract **- High speed designs with controlled impedance traces need to have the trace line width calculated as a function of the board cross section. Allegro can do these calculations if the cross section form is filled out correctly.**

When we started using the Cadence impedance calculator we got significantly different values than what were shown in the stackup and impedance specifications developed using Polar Instruments software and verified by our board vendor.

This paper describes how we fill out the Allegro cross section form to achieve correlation with the specification.

I. Basic Trace Structures

There are two basic trace types used for controlled impedance– traces-stripline and microstrip.

A stripline is a trace on an inner layer with a plane above and below it. Fig. 1 shows an "offset" stripline since the conductor is not in the center of the dielectric.

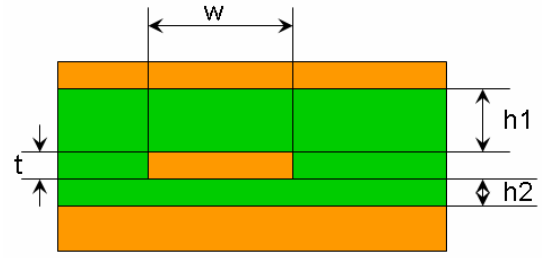

Fig. 1 Offset Stripline

Microstrip, shown in Fig.2. is a trace on the outside of the board with a plane below it.

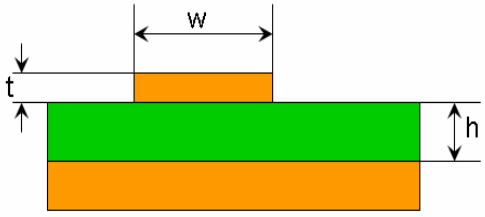

Fig. 2 Microstrip

For differential pairs, two coupled traces are used, either edge coupled or broadside coupled in either of these structures.

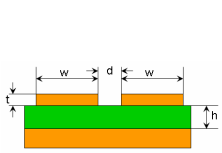

Fig. 3 Edge

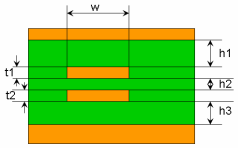

Fig. 4 Broadside

II. Allegro Cross Section Form

The Allegro cross section form has two different formats. The default format for Allegro Design Expert looks like Fig. 5, (next page) whereas the default format of Allegro PCB SI, called the "modern" format, looks like Fig. 6. Notice that the modern format has columns for material parameters and impedance calculations. Setting the "xsection_modern" variable in the "Misc" category of the User Preferences Editor causes Allegro Expert to use the modern format. Allegro must be restarted to activate this. Note that "Differential Mode" must be unselected to see the materials column in the modern format (Fig. 7).

III. Materials

Selecting a material populates the material parameters for that layer of the design Or directly enter the parameters into the form.

The default selection of materials is defined in the *materials.dat* file found in folders defined in the "materialpath" variable. The default for this is:

```
. (board directory)
$HOME/pcbenv
$CDSROOT/share/local/pcb
$CDSROOT/share/pcb/text
```

With CDS_SITE set the third entry changes.

```
. (board directory)
$HOME/pcbenv
$CDS_SITE/pcb
$CDSROOT/share/pcb/text
```

Setup->Materials from the Allegro menu, open an editor for the *materials.dat* file which saves the file in the same directory as the board. A text editor can be used to create *materials.dat* without starting Allegro.

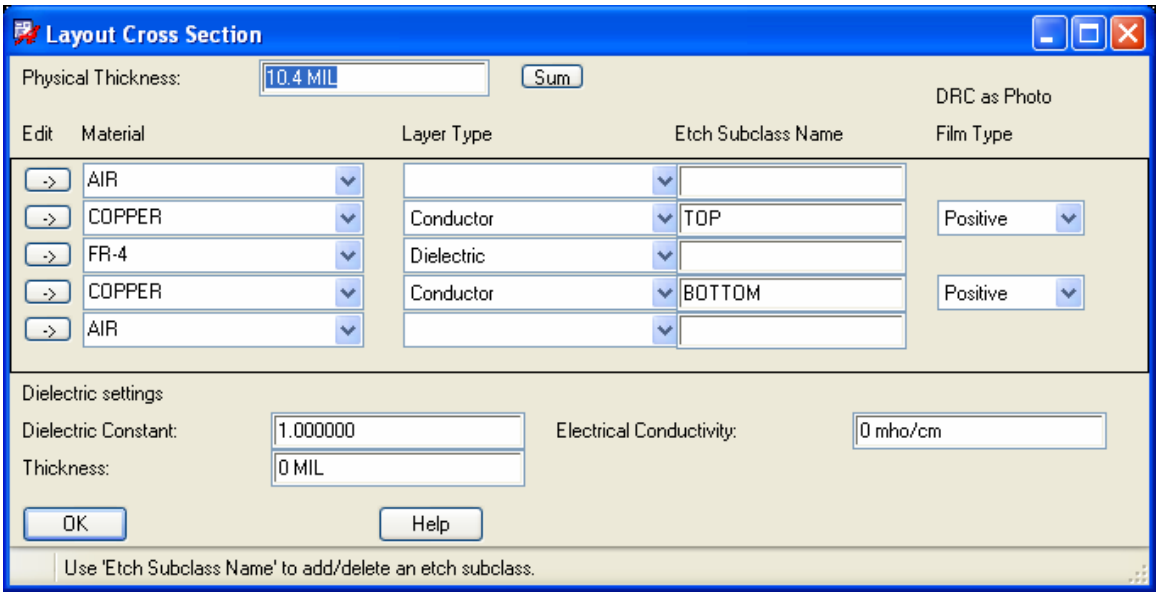

Fig. 5 Classic Cross Section Form

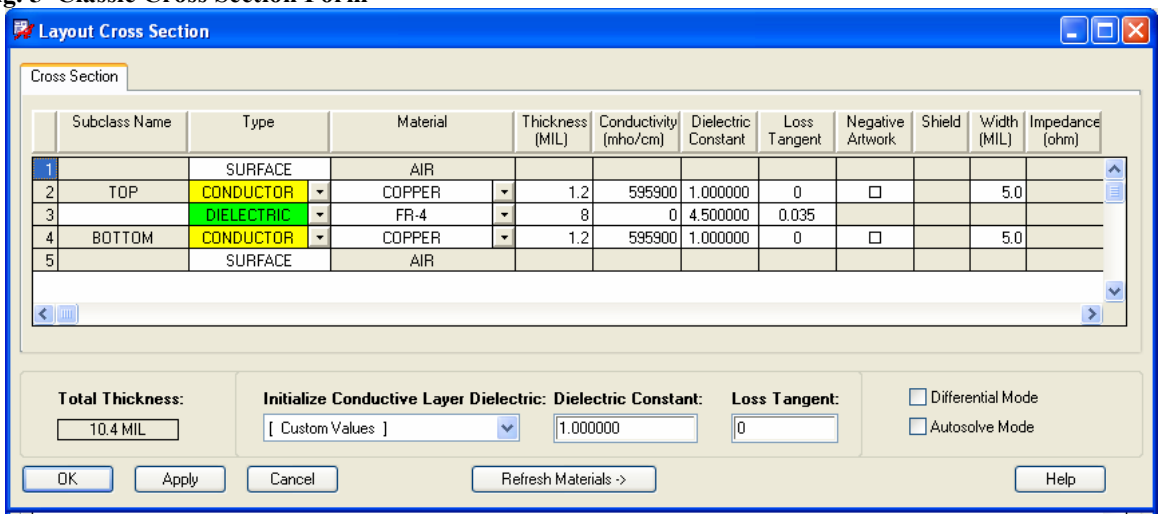

Fig. 6 Modern Cross Section Form

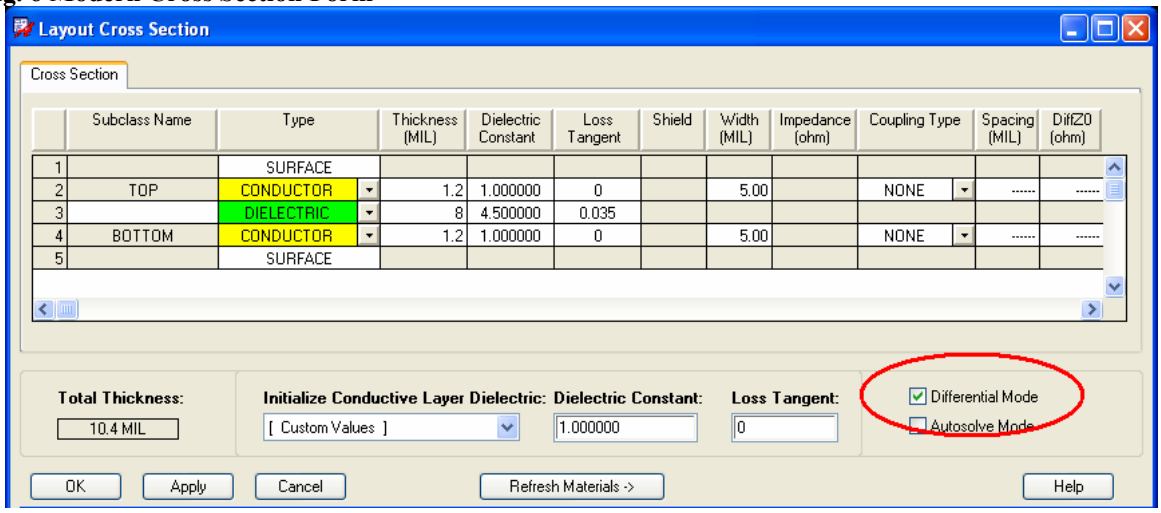

Fig. 7 Modern Cross Section Form with Differential Mode Selected

Meaningful material names, like "COPPER_1_OZ" or "FR-4_4MIL" can make the cross section form be descriptive and easy to setup. It also allows the creation of a simple cross section report generator. By having only approved materials in the *materials.dat* file, errors caused by specifying unavailable materials or thicknesses are reduced.

For boards that have outer layers created by an additive process ("foil with plating up"), the user can define specific dielectrics and conductors for that. However two adjacent conductor layers can not be specified so the thickness of the copper foil and the plating must be combined into a single conductor.

Dielectric names that differentiate between "core" (with copper on one or both sides) and "pre-preg" to can be created further define the construction of the board.

IV. Conductive Layer Dielectric

At the bottom of the cross section dialog is a box titled *Initialize Conductive Layer Dielectric.*

Fig. 8 Detail of Cross Section Dialog

At first thought this seems wrong – specifying the dielectric for a conductor is meaningless. This specifies the parameters for the dielectric material that flowed into the area beside conductors, i.e. the pre-preg circled in in Fig. 9. Setting this is essential for good impedance calculations.

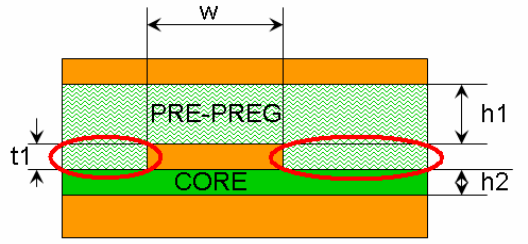

Fig. 9 Dielectric Beside Conductor

Select a material from the pull-down menu in this section, to set the parameters for all conductors in the main setup table. If there are different dielectric constants on various conductor layers, such as pre-preg layers having different dielectric constants, the values for each conductor layer will have to manually entered. This is a case where having meaningful dielectric names is helpful. The parameters from the adjacent pre-preg layer can be used for the conductor layer..

V. Trapezoidal Shape

To get good correlation between Allegro and the Polar Instruments calculations we found that it was necessary to specify trapezoidal traces. This is the typical shape of a trace that has been built up during the etch/plating process.

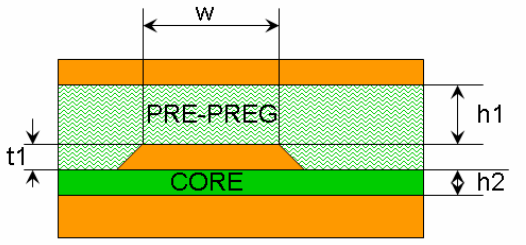

Fig. 10 Trapezoidal Trace

Trapezoid traces are specified by setting the *trapezoidal_angle_in_degrees* variable in the "Signal Analysis" category of the User Preferences dialog. I used "74" as suggested in SourceLink solution 11064512.

VI. Solder Mask

Experienced SI engineers know that solder mask on a board affects the impedance. To get good impedance calculations layers on the outside of the board representing the solder mask must be added. Adding a material in the *materials.dat* file is useful here.

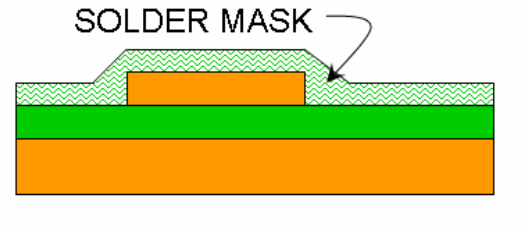

Fig. 11 Solder Mask

The thickness for the solder mask, which is typically conformal, can't be accurately represented in the cross section setup since Allegro assumes that the dielectric which flowed around the conductors is the same thickness as the conductors and that the dielectric above a conductor covers the whole area of the board. However it seems that specifying solder mask dielectric for the outer conductor layers and for the specified thickness for the solder mask layer itself (with the correct thickness) is a good approximation. The error is primarily at the very edge of the conductor traces.

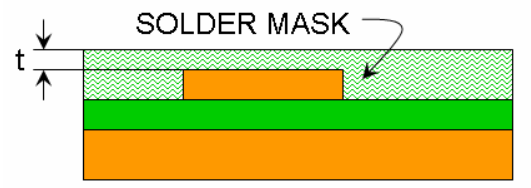

Fig. 12 Solder Mask as Specified

VII. Difference between Cadence vs. Polar measurements

The Polar Instruments software measures the thickness of the pre-preg dielectric from the core dielectric to the adjacent core dielectric (left side of Fig. 13) whereas Cadence measures it from copper to copper (right side of Fig. 13).

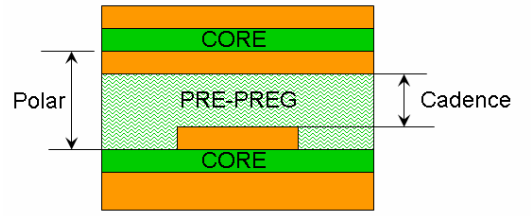

Fig. 13 Polar vs. Cadence Thickness

This difference must be accounted for when specifying the dielectric thickness in the cross section definition.

VIII. Line Widths

The line width calculated using field solver equations based on the board cross section usually result in widths that are not standard manufacturing widths. Most fabricators have a resolution of 0.25 mils for line widths. If the width calculator comes up with 4.65 mils, the value should be set to either 4.5 or 4.75 mils. This small difference is well within the typical impedance tolerance.

IX. Cross Section Report

The tech file can be used to create a cross section report from an Allegro design. Within the tech file are a series of sections for each layer of the cross section listing the fields from the cross section form. (The impedance values are not listed because they are calculated values, not parameters.). This data can be used to create a simple report. If the materials are defined with informative names, the report is more informative.

```
Lyr# Type        Material        Thickness
0    SURFACE     AIR               0.00
1    DIELECTRIC  CONFORMAL_COAT    0.40
2    CONDUCTOR   COPPER            2.20
3    DIELECTRIC  NELCO_4000_13     3.20
4    PLANE       COPPER            0.60
5    DIELECTRIC  NELCO_4000_13     5.00
6    CONDUCTOR   COPPER            0.60
7    DIELECTRIC  NELCO_4000_13     4.50
8    CONDUCTOR   COPPER            0.60
9    DIELECTRIC  NELCO_4000_13     5.00
```

Fig. 13 Example of a cross section report

X. Validation

To verify that the Cadence impedance calculator gives the expected results, we filled out the Allegro cross section dialog using the cross section and impedance specification for a design. We then calculated the line width for the various impedances specified. These were compared to the specified line widths and to those calculated by Polar Instruments software.

Using the techniques and settings described above, we achieved correlation within 50% of the specified tolerance. Part of the cross section and impedance specification for that board are shown in Fig.s 14 and 15. The correlation results are summarized in Table 1. In most cases we got the same value–the difference being due to which way the round-off to 0.25 mils was done.

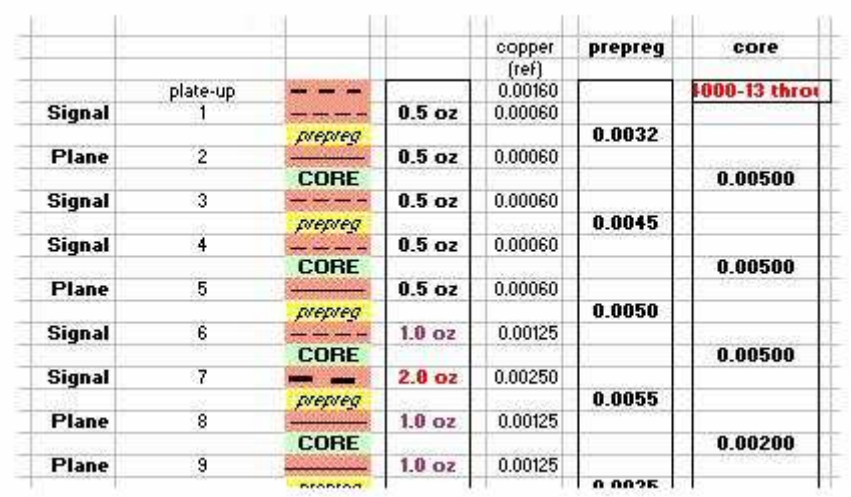

Fig. 14 Partial Cross Section Specification

Impedance Table

	Ref layer (s	Line	Space	Nominal Imp	Tolerance	Type
Layer 1	2	0.00575	N/A	50	12	Single
		0.00525	0.01100	100	15	Diff
Layer 3	2 & 5	0.00700	N/A	50	10	Single
		0.00625	0.00975	100	12	Diff
Layer 4	2 & 5	0.00700	N/A	50	10	Single
		0.00625	0.00975	100	12	Diff
Layer 6	5 & 8	0.00725	N/A	50	12	Single
		0.00600	0.01000	100	12	Diff
Layer 7	5 & 8	0.00700	N/A	50	15	Single

Fig. 15 Partial Impedance Specification

Value From Specification							Polar	CDS	CDS	%Error vs.	
Lyr	Ref	Z0	Tol.	Gap	Type	Width	Width	Width	Adj.	Spec	Polar
1	2	50	12%	N/A	Single	5.75	5.9	5.84	5.75	0%	-3%
		100	15%	11	Diff	5.25	5.3	5.15	5.25	0%	-1%
3	2&5	50	10%	N/A	Single	7	7	7.03	7	0%	0%
		100	12%	9.75	Diff	6.25	6.5	6.41	6.5	4%	0%
4	2&5	50	10%	N/A	Single	7	7	7.03	7	0%	0%
		100	12%	9.75	Diff	6.25	6.25	6.41	6.5	4%	4%
6	5&8	50	12%	N/A	Single	7.25	7	7.06	7	-3%	0%
		100	12%	10	Diff	6	6	6.12	6	0%	0%
7	5&8	50	15%	N/A	Single	7	6.25	6.61	6.5	-7%	4%
10	9&12	50	10%	N/A	Single	4.75	4.9	4.82	4.75	0%	-3%
11	9&12	50	10%	N/A	Single	4.75	4.9	4.82	4.75	0%	-3%

Table 1 Comparison of Line Width Calculations