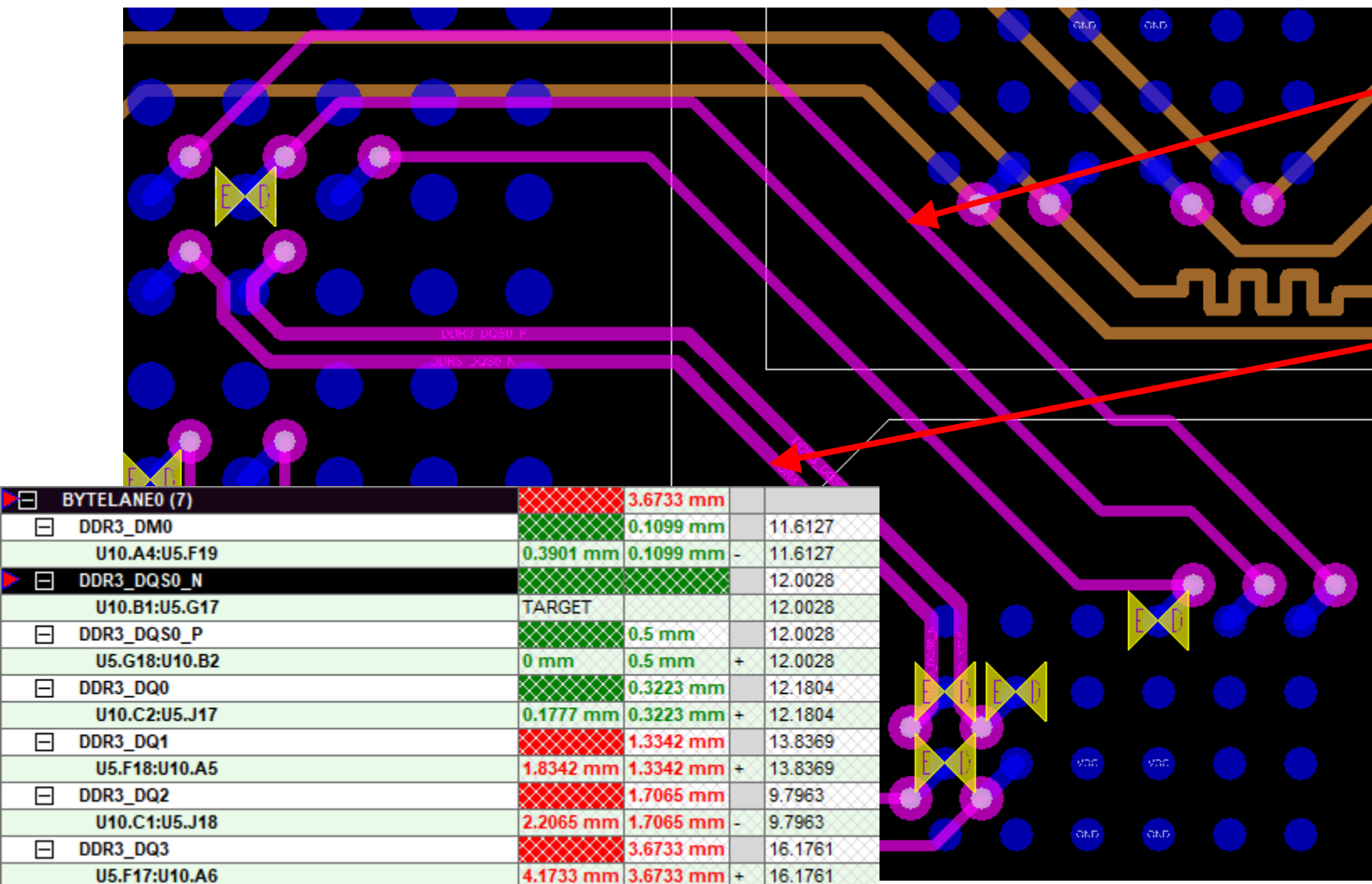Target – Longest routed member

RDly −5.8798

Heads up display showing margin between Target and RPD member shown in Constraint Manager

DDR3_DQ2		5.8798 mm
U10.C1:U5.J18	6.3798 mm	5.8798 mm

Longest routed member but user defined Target set to one half of the Differential Pair.

`T RDly -3.6733    +1.7065`

Target value shorter than longest routed RPD member. When Add Delay command on the Target the Heads-up display shows: T you are adding delay to the Target. The T value (-3.6733) is the distance to match the longest net within tolerance and the Rdly Value (+1.7065) is the Matched Group worse case margin.

BYTELANE0 (7)		3.6733 mm		
DDR3_DM0		0.1099 mm		11.6127
U10.A4:U5.F19	0.3901 mm	0.1099 mm	-	11.6127
DDR3_DQS0_N				12.0028
U10.B1:U5.G17	TARGET			12.0028
DDR3_DQS0_P		0.5 mm		12.0028
U5.G18:U10.B2	0 mm	0.5 mm	+	12.0028
DDR3_DQ0		0.3223 mm		12.1804
U10.C2:U5.J17	0.1777 mm	0.3223 mm	+	12.1804
DDR3_DQ1		1.3342 mm		13.8369
U5.F18:U10.A5	1.8342 mm	1.3342 mm	+	13.8369
DDR3_DQ2		1.7065 mm		9.7963
U10.C1:U5.J18	2.2065 mm	1.7065 mm	-	9.7963
DDR3_DQ3		3.6733 mm		16.1761
U5.F17:U10.A6	4.1733 mm	3.6733 mm	+	16.1761

T Value: Longest Pin Pair DQ3 minus the tolerance, minus the current length of the Target (16.1761 – 0.5) – 12.0028 = -3.6733
Rdly Value: margin between the Target and the shortest pin pair DQ2 minus the tolerance (12.0028 – 0.5) – 9.7962 = 1.7065