**Area**: Analog Mixed Signal

**Specific Area**: VHDL view and symbol creation

**Error Message**: xmvhdl\_p: \*F,NOLSTD: logical library name STD must be mapped to a design library

**Description:** I am doing AMS verification for a RX Path. A vhdl code is already present for rx\_resampler block. To perform the AMS test, a view and a symbol of rx\_resampler block is required. I have used two options to create the view.

1. Library Manager🡪File🡪New🡪cellview



Getting error at the time of extract (File🡪Extract)

Error file: 

1. Library Manager🡪File🡪New🡪cellview



Error file: 