Revision April 2009

PEX86[13_14_15_17_18_19] GEN2 SERDES HSPICE Model

NOTICE

This Hspice package is a self-contained GEN2 SERDES simulation directory that represents the Hspice model for Transmit and Receive circuitry for the 8613, 8614, 8615, 8617, 8618, and 8619 PCI-Express interface (324BGA).

1. "io.sp"

The main SPICE deck in which the user can change simulation corner and modify selectable input signals:

```
**********************
1A. Process Variation.
**********************

Example of how to specify slow, typical, or fast process corner:

.lib './process_corner.lib' ss
.lib './process_corner.lib' tt
.lib './process_corner.lib' ff

*****************************
1B. Voltage Supply Variation.
*****************************

To specify voltage variation, set vdd to a range of 0.95V-1.1V

vvdd vdd 0  dc 1.0
```

****
1C. TX Control Inputs
****

The following 2 registers (DRV_LVL[4:0] and EMP_POST4:0]) control the TX Drive Level as well as the De-Emphasis levels according to the table below which shows all the possible combinations that yield a minimum of 800mV transition amplitude. Of these combinations, only certain values yield the appropriate 3-4dB or 5.5-6.5dB equalization which is highlighted in green.

Note: These values are based on a typical GEN2 package driving into 50Ω load. Actual values for this particular package part may vary slightly. Users are encouraged to simulate using the provided s-parameter package models to obtain the most accurate values.

EMP_PST [4:0] Hex	DRV_LVL [4:0] Hex	Transition Amplitude (mV)	Non-Transition Amplitude (mV)	Equalization (dB)
1	11	820	789	0.34
1	12	849	818	0.33
1	13	876	845	0.31
2	10	799	742	0.65
2	11	830	773	0.61
2	12	858	802	0.58
2	13	884	829	0.56
3	10	809	727	0.93
3	11	839	758	0.88
3	12	867	787	0.84
3	13	893	814	0.80
4	10	818	712	1.22
4	11	848	743	1.15
4	12	876	772	1.09
4	13	901	799	1.04
5	F	797	664	1.59
5	10	828	697	1.50
5	11	857	728	1.41
5	12	884	758	1.34
5	13	909	785	1.27

5	1F	796	663	1.59
6	F	806	649	1.88
6	10	837	682	1.77
6	11	866	714	1.68
6	12	892	743	1.59
6	13	916	770	1.51
6	1F	806	649	1.88
7	F	816	635	2.18
7	10	846	668	2.05
7	11	874	700	1.94
7	12	900	729	1.83
7	13	924	756	1.74
7	1F	816	635	2.18
8	F	825	620	2.48
8	10	855	654	2.33
8	11	883	685	2.20
8	12	908	715	2.08
8	13	931	742	1.98
8	1F	825	620	2.47
9	E	802	571	2.95
9	F	834	607	2.77
9	10	863	640	2.60
9	11	891	671	2.46
9	12	916	701	2.33
9	13	938	728	2.21
9	1E	802	571	2.96
9	1F	834	606	2.77
A	E	811	557	3.27
A	F	843	593	3.06
A	10	872	626	2.88
A	11	899	658	2.71
A	12	923	687	2.57
A	13	945	714	2.43
A	1E	811	557	3.27
A	1F	843	593	3.06
B	E	821	543	3.58
B	F	851	579	3.35
B	10	880	612	3.15
B	11	906	644	2.97
B	12	930	673	2.81
B	13	951	700	2.66
B	1E	820	543	3.58
B	1F	851	579	3.35
C	D	797	492	4.19

C	E	829	530	3.89
C	F	860	566	3.64
C	10	888	599	3.42
C	11	914	630	3.22
C	12	937	660	3.05
C	13	958	687	2.89
C	1D	797	492	4.19
C	1E	829	530	3.89
C	1F	860	565	3.64
D	D	806	479	4.52
D	E	838	517	4.20
D	F	868	552	3.93
D	10	896	586	3.69
D	11	921	617	3.48
D	12	944	646	3.29
D	13	964	673	3.11
D	1D	806	479	4.52
D	1E	838	516	4.20
D	1F	868	552	3.93
E	D	815	466	4.86
E	E	847	503	4.51
E	F	876	539	4.22
E	10	903	572	3.96
E	11	928	604	3.73
E	12	950	633	3.53
E	13	970	660	3.34
E	1D	815	466	4.86
E	1E	846	503	4.52
E	1F	876	539	4.22
F	D	824	453	5.20
F	E	855	490	4.83
F	F	884	526	4.51
F	10	911	559	4.23
F	11	935	591	3.98
F	12	957	620	3.76
F	13	975	647	3.56
F	1D	823	453	5.20
F	1E	855	490	4.83
F	1F	884	526	4.51
10	C	799	399	6.02
10	D	832	439	5.55
10	E	863	477	5.15
10	F	892	513	4.81
10	10	918	546	4.51

10	11	942	578	4.25
10	12	963	607	4.01
10	13	981	634	3.79
10	1C	799	399	6.02
10	1D	832	439	5.55
10	1E	863	477	5.15
10	1F	892	513	4.81
11	C	808	387	6.40
11	D	841	427	5.89
11	E	871	464	5.46
11	F	899	500	5.10
11	10	925	533	4.78
11	11	948	565	4.50
11	12	969	594	4.24
11	13	986	621	4.02
11	1C	808	387	6.40
11	1D	840	427	5.89
11	1E	871	464	5.46
11	1F	899	500	5.10
12	C	816	374	6.77
12	D	849	414	6.23
12	E	879	452	5.78
12	F	906	487	5.39
12	10	932	521	5.05
12	11	954	552	4.75
12	12	974	582	4.48
12	13	991	609	4.24
12	1C	816	374	6.78
12	1D	849	414	6.23
12	1E	879	452	5.78
12	1F	906	487	5.39
13	C	825	362	7.16
13	D	857	402	6.58
13	E	886	439	6.09
13	F	913	475	5.68
13	10	938	509	5.32
13	11	960	540	5.00
13	12	980	569	4.72
13	13	996	596	4.46
13	1B	795	326	7.76
13	1C	825	362	7.16
13	1D	856	402	6.58
13	1E	886	439	6.09
13	1F	913	475	5.68

14	B	799	308	8.29
14	C	833	350	7.54
14	D	864	389	6.93
14	E	893	427	6.41
14	F	920	463	5.97
14	10	944	496	5.59
14	11	966	528	5.25
14	12	985	557	4.95
14	13	1001	584	4.68
14	1B	804	313	8.19
14	1C	833	349	7.54
14	1D	864	389	6.93
14	1E	893	427	6.41
14	1F	920	463	5.97
15	B	808	296	8.73
15	C	841	337	7.93
15	D	872	377	7.28
15	E	901	415	6.73
15	F	927	451	6.26
15	10	950	484	5.86
15	11	972	516	5.50
15	12	990	545	5.19
15	13	1006	572	4.90
15	1B	812	301	8.62
15	1C	841	337	7.93
15	1D	872	377	7.28
15	1E	900	415	6.73
15	1F	927	451	6.26
16	B	816	284	9.18
16	C	849	326	8.32
16	D	879	365	7.63
16	E	907	403	7.05
16	F	933	439	6.56
16	10	956	472	6.13
16	11	977	504	5.76
16	12	995	533	5.42
16	13	1010	560	5.12
16	1B	820	289	9.05
16	1C	849	325	8.33
16	1D	879	365	7.63
16	1E	907	403	7.05
16	1F	933	439	6.56
17	B	824	272	9.63
17	C	856	314	8.72

17	D	886	354	7.98
17	E	914	391	7.37
17	F	939	427	6.85
17	10	962	460	6.40
17	11	982	492	6.01
17	12	999	521	5.65
17	13	1014	548	5.34
17	1B	828	277	9.50
17	1C	856	314	8.72
17	1D	886	353	7.99
17	1E	914	391	7.37
17	1F	939	427	6.85
18	A	798	216	11.35
18	B	832	260	10.10
18	C	864	302	9.13
18	D	893	342	8.35
18	E	921	380	7.70
18	F	945	415	7.15
18	10	968	449	6.68
18	11	987	480	6.26
18	12	1004	509	5.89
18	13	1018	537	5.56
18	1A	802	222	11.16
18	1B	836	266	9.96
18	1C	864	302	9.13
18	1D	893	342	8.35
18	1E	921	379	7.70
18	1F	945	415	7.15
19	A	806	204	11.91
19	B	840	249	10.57
19	C	871	290	9.54
19	D	900	330	8.71
19	E	927	368	8.02
19	F	951	404	7.45
19	10	973	437	6.95
19	11	992	469	6.51
19	12	1008	498	6.12
19	13	1021	525	5.78
19	1A	810	210	11.71
19	1B	844	254	10.42
19	1C	871	290	9.54
19	1D	900	330	8.71
19	1E	927	368	8.03
19	1F	951	404	7.45

1A	A	814	193	12.49
1A	B	847	237	11.05
1A	C	878	279	9.95
1A	D	907	319	9.08
1A	E	933	357	8.35
1A	F	957	392	7.74
1A	10	978	426	7.22
1A	11	996	457	6.76
1A	12	1012	487	6.36
1A	13	1025	514	6.00
1A	1A	818	199	12.28
1A	1B	851	243	10.89
1A	1C	878	279	9.96
1A	1D	907	319	9.08
1A	1E	933	357	8.35
1A	1F	957	392	7.74
1B	A	821	182	13.09
1B	B	854	226	11.55
1B	C	885	268	10.38
1B	D	913	308	9.45
1B	E	939	346	8.68
1B	F	962	381	8.04
1B	10	983	415	7.50
1B	11	1000	446	7.01
1B	12	1016	475	6.59
1B	13	1028	503	6.22
1B	1A	826	188	12.86
1B	1B	858	232	11.38
1B	1C	885	268	10.38
1B	1D	913	308	9.45
1B	1E	939	345	8.69
1B	1F	962	381	8.04
1C	A	829	171	13.71
1C	B	861	215	12.06
1C	C	892	257	10.81
1C	D	919	297	9.82
1C	E	945	334	9.02
1C	F	967	370	8.35
1C	10	987	404	7.77
1C	11	1004	435	7.27
1C	12	1019	464	6.83
1C	13	1031	491	6.44
1C	19	799	131	15.71
1C	1A	833	177	13.46

1C	1B	865	221	11.87
1C	1C	891	257	10.81
1C	1D	919	297	9.83
1C	1E	944	334	9.02
1C	1F	967	370	8.35
1D	9	802	114	16.95
1D	A	836	160	14.36
1D	B	868	204	12.58
1D	C	898	246	11.25
1D	D	925	286	10.20
1D	E	950	324	9.36
1D	F	972	359	8.65
1D	10	992	393	8.05
1D	11	1008	424	7.52
1D	12	1022	454	7.06
1D	13	1034	481	6.65
1D	19	806	120	16.55
1D	1A	841	166	14.09
1D	1B	872	210	12.38
1D	1C	898	246	11.25
1D	1D	925	286	10.21
1D	1E	950	323	9.36
1D	1F	972	359	8.65
1E	9	809	103	17.90
1E	A	843	149	15.04
1E	B	875	193	13.11
1E	C	904	235	11.69
1E	D	931	275	10.59
1E	E	955	313	9.69
1E	F	977	349	8.95
1E	10	996	382	8.32
1E	11	1012	413	7.77
1E	12	1025	443	7.29
1E	13	1037	470	6.87
1E	19	814	109	17.44
1E	1A	848	155	14.74
1E	1B	879	199	12.90
1E	1C	904	235	11.70
1E	1D	931	275	10.59
1E	1E	955	313	9.70
1E	1F	977	348	8.95
1F	9	817	93	18.91
1F	A	850	139	15.75
1F	B	881	183	13.66

1F	C	910	225	12.15
1F	D	936	265	10.98
1F	E	960	302	10.04
1F	F	981	338	9.26
1F	10	999	371	8.60
1F	11	1015	403	8.03
1F	12	1028	432	7.53
1F	13	1039	459	7.09
1F	19	821	99	18.40
1F	1A	854	145	15.43
1F	1B	885	188	13.44
1F	1C	910	225	12.15
1F	1D	936	264	10.98
1F	1E	960	302	10.04
1F	1F	981	338	9.26

Notes:

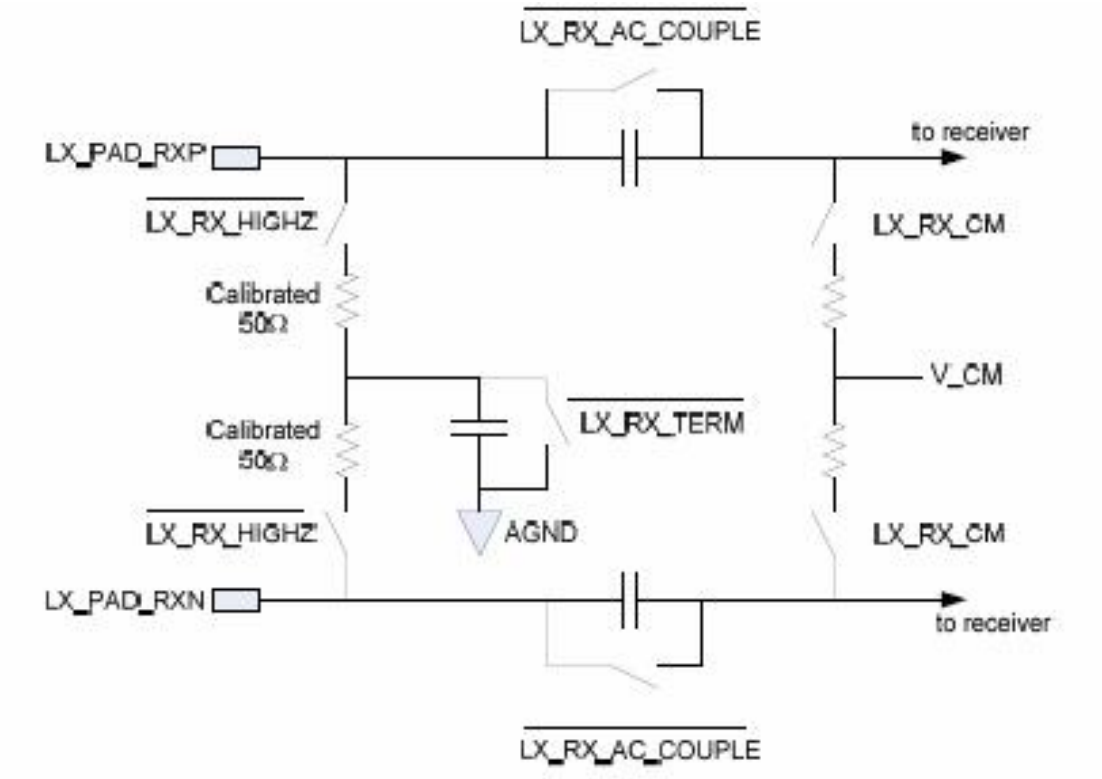
1. All levels are based on TX package driving straight into 50Ω termination through 0.1uF cap with Vdd supply at 1v.

Examples of default 3.5dB & 6dB setting:

Mode	Drive Level	De-Emphasis	dB Equalization
3.5dB	10'h (896mV)	0D'h (586mV)	20*log[(896/586)] = 3.69dB
6.0dB	0E'h (901mV)	15'b (415mV)	20*log[(901/415)] = 6.73dB

****
1D. RX Control Inputs
****

The following bits control the RX settings:



RX_EQ[3:0] programs the receive equalization mode per table below:

RX_EQ[3:0] {HEX}	Receive Equalization
0 (Default)	Off
1'h	Minimum Equalization (Recommended)
2'h-5'h	Low Equalization
3'h-6'h	Low Medium Equalization
7'h-9'h	Medium Equalization
A'h-D'h	High Medium Equalization
E'h-F'h	Maximum Equalization

RX_TERM – RX Termination Enable

RX_TERM	Mode
0	Enable 50Ω internal termination (Recommended)
1	Disable 50Ω internal termination

RX_CM – RX Common-Mode Enable

RX_CM	Mode
0	Disable RX internal common mode
1	Enable RX internal common mode (Recommended)

RX_AC_COUPLE – RX AC Couple Enable

RX_AC_COUPLE	Mode
0	Enable RX internal AC coupling cap
1	Disable RX internal AC coupling cap (Recommended)

****
1E. TX/RX Control Inputs
****

BAND - GEN-I vs. GEN-II Speed Selector

BAND	Mode
0	GEN2 5Gbps
1	GEN1 2.5Gbps

RES_CODE[3:0] - Resistor Code for 50 ohm calibrated impedance.

RES_CODE[3:0]	Mode
1100'b	SS Process
0111'b	TT Process
0001'b	FF Process

2."txrx_sparam_system.spi"

This file represents the top level system level netlist which instantiates Tx transmit, Rx Receive, package (S-Parameter) and transmission line. User can modify this file to:

- Select either TX7 or TX6 package model.
- Specify customer specific FR4 channel models.
- Specify customer specific AC coupling capacitor value.

The following files (3-11) are to be used as is. No edits or modifications by the user is allowed or recommended.

3."hspice_drvr_rcvr_pcx.inc"{Instantiated in txrx_system.spi}

This file contains all the low level transistor netlist for TX/RX in encrypted format. Sub-circuits TX and RX

represent the top level transmit-receive blocks. They are called out independently and separately. User can swap either TX or RX to simulate with non-PLX component(s).

4. **"netlist_tx_rx.inc"** {Instantiated in txrx_system.spi}

This file contains the top level netlist topology of RX/TX. User must follow the pin sub-circuit pin-ordering when instantiating TX & RX.

5. **"pex8618_tx6_rx6_tx5.s14p"** {Instantiated in txrx_sparam_system.spi}

S-Parameter model of 324 PBGA wire-bond package which includes lanes TX7, TX6, and RX6.

An additional s-parameter file is also available that models additional RX[4-5] and TX[4-5] lanes:

(pex8618_tclk_tx4_tx5.s20p)

6. **"process_corner.lib"**

These are the pointers to the TSMC's 90nm SPICE models. Users should use appropriate setting for process variation in io.sp file.

Note: The following transistor names are used and therefore reserved for
PLX SERDES: nch, pch, nch_hvt, pch_hvt. If PLX Tx/Rx are simulated with other non-PLX circuitry, care must be taken to rename transistor model names differently to avoid naming conflicts.

7. **"cln90g_lk_resmodel.inc"**

This file includes the encrypted SPICE model file provided by TSMC for 90nm process.

8."channel.inc/p5.rlc"

This file contains sample electrical model of PCB environment. Users should specify their own channel models.

9."86xx_serdes_topology.jpg"

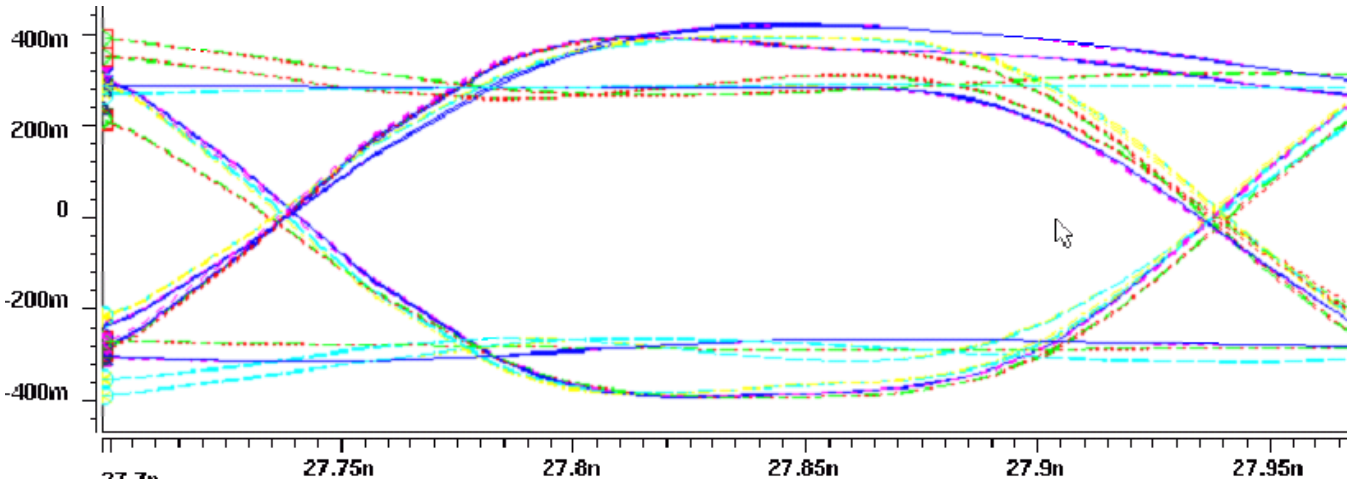
Graphical view of the Tx, Rx, and package sub-circuit instantiation.

10. "eye_rxpin6_diff.inc"

This file generates 100UI samples of RX eye. User can increase the number of UI sample points beyond 100 at the expense of more simulation time.

11. "io.sav/diff[11-110]_rx6.cfg"

This configuration file can be loaded from Avanwave tool (Configuration -> Open) to load the RX eye pattern.



12. "io.tr0"

This file is a sample transient output file for reference.