Guidelines/Strategies for Routing Success

a.k.a

Minimization of 'Post Route Traumatic Stress Syndrome'

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Post-traumatic route syndrome can happen to anyone. It is that sick feeling you get when you think you have a board routed and then discover a major problem that could have been prevented and worst case causes you to reroute. It almost always occurs when there has not been enough time spent in pre-route preparation. As with any other affliction, 'an ounce of prevention is worth a pound of cure'. Listed below are a few things to keep in mind before beginning your route and during the routing process.

What Should I Do First?

Prior to embarking on any routing scheme you should first verify:

- All physical and spacing rule sets have been entered, i.e…
  - Routing and fanout Vias added to 'Current Via List'
  - Line widths entered
  - Nets assigned to classes and assignment tables have been completed.
  - PWR/GND nets assigned to unique Physical rule set(s)
- All routing rules have been applied via Constraint Manager.
- The Cross-section is entered and correct.
- Routing and placement keepouts have been defined.
- Required DRC modes have been turned on.
- Review placement for ease of route/fanout, prefer components to be placed on .005" or .001" grid.

Determine What Methodology Will Be Used to Control Crosstalk

- Crosstalk is generally controlled by either 1 or 2 methods. One method is to set parallelism rules in CM and the other is to define crosstalk parallel and adjacent segment rules within a Specctra .do file. Consideration must be given for both same and adjacent (Tandem) layer analysis as well as whether or not the checks will be by-segment or cumulative. The SI engineer ultimately determines what techniques will be used for any given board.

Translation to Specctra

- It is preferred that translation to Specctra be accomplished through the, "File => Export => Specctra" pull-down menu. Especially if the time to be spent routing in Specctra is anticipated to be significant. Alternately, for small routing changes, the 'Specctra' translation button available in the Allegro GUI can be also used.

Do Files

- Every board should have a minimum of 3 Do files. Two of which are automatically generated by exporting to Specctra, 'board_name_***rules***.do' and 'board_name_***forget***.do', and one user created do file named, '***master.do'*** file. The rules.do and master.do files should normally always be applied before beginning the route process.

What's in the Master.do File?

Examples of commands commonly found in the master.do file are:

set same_net_checking on
experienced users may toggle this on/off
rule pcb (accordion_gap .020)
gap value may vary by board or class
rule pcb (trombone_gap .020)
gap value may vary by board or class
rule pcb (patterns_allowed meander trombone accordion)
set average_pair_length off
bestsave on $/brd_best.w
rule PCB (clearance .010 (type smd_via_same_net))
this value may vary by board but should never be less than .010
set turbo_stagger on
optional for designs with staggered PGAs
set selfcouple on
prevents self-coupling in elongation patterns

```
rule pcb  (parallel_segment (gap .007) (limit .72))
rule pcb  (parallel_segment (gap .008) (limit .92))
rule pcb  (parallel_segment (gap .009) (limit 1.17))
rule pcb  (parallel_segment (gap .010) (limit 1.5))
rule pcb  (parallel_segment (gap .011) (limit 1.9))
rule pcb  (parallel_segment (gap .012) (limit 2.4))
#
rule pcb  (tandem_segment (gap .003) (limit .3))
rule pcb  (tandem_segment (gap .004) (limit .4))
rule pcb  (tandem_segment (gap .005) (limit .5))
rule pcb  (tandem_segment (gap .006) (limit .6))
rule pcb  (tandem_segment (gap .007) (limit .7))
rule pcb  (tandem_segment (gap .008) (limit .8))
rule pcb  (tandem_segment (gap .009) (limit .9))
rule pcb  (tandem_segment (gap .010) (limit 1.0))
rule pcb  (tandem_segment (gap .011) (limit 1.1))
rule pcb  (tandem_segment (gap .012) (limit 1.2))
rule pcb  (tandem_segment (gap .013) (limit 1.3))
```

Board level, per segment , crosstalk control. Actual values to be provide by SI engineering.

```
area add_pt 9.769 3.031
area add_pt 11.041 3.031
area add_pt 11.041 2.052
area add_pt 9.393 2.052
area close_poly
define (region region1 (digitize (layer signal)))
rule region region1 (clearance .005 (type wire_wire))
rule region region1 (clearance .005 (type via_wire))
rule region region1 (width .0045)
```

Routing Region definition and associated clearance rules. Actual values to be provided by SI and/or mechanical engineering.

Note, if Areas are defined in Allegro, The associated Regions are automatically added to the translated Specctra *.dsn file

Identify Your Board's Unique Routing Requirements.

- Prior to routing it is important to do a thorough evaluation of the board to determine the types of routing requirements that must be achieved. Some items that may require special handling are:
    - Differential Pairs
    - Tightly matched (+/- .005) wire/net lengths
    - Buss routing, No vias allowed
    - 45 degree wire bends
    - Wire bend count limits
    - Wires/Nets with length rule requirements that are less than Manhattan.
    - Buried Vias
    - Virtual Pins
    - ?????????

Ensure Component Placement is as Good as it Can Be.

- Good component placement is mandatory to achieve favorable routing results. Extra consideration should be given to all components that are connected via virtual pairs to ensure that the pins of the pair are in close proximity to each other. Additionally there should be enough room between components to allow for fanout vias.

Evaluate Component Placement versus Length Rules

- Ideally, there should be no nets/wires that impose Max length rules that are less than the Manhattan distance between pins. In order to identify these conditions the, 'Place Length' report should be run in *Specctra, Report => Specify => Place Length.* This report will texturally and graphically identify all wires/nets that have max length rules that are less than the Manhattan length. If there are Place Length violations, you should first attempt to adjust placement to accommodate the max length rule. If all placement options have been exhausted, you then should confer with board's SI engineer to find out if the Max length rules that have been applied can be increased to eliminate the Manhattan Place Length Error. If not, you will more than likely need to manually pre-route all of the remaining wire/nets that have Place Length rule violations.

Fan it Out!

Before starting internal signal layer routing, ensure that fanout has been completed for all SMD/BGA pins.

- Ensure the designated fanout via has been selected and all other routing vias are unselected.

Upon completion of fanout:

- protect all routing by layer , i.e.., ***'protect layer_wires TOP BOTTOM'*** and save a route (*.rte) file of the protected fanouts.
- Unselect the fanout via and select the preferred routing via(s).

- Translate back to Allegro and turn on layer "NO_PROBE_BOTTOM" and check if any vias need to be moved. Move vias if required.
- Inform the DFT group that the initial breakouts are complete and ready for testability evaluation.

Push the Smart Route Button

- Although most of our boards cannot be fully auto-routed, there are still benefits from seeing where/what items appear to be problematic for the router. Running Smart Route can often uncover spacing, keepout, trace width, types of problems that had previously gone unnoticed. The typical smart route should be run with the following options:
  smart_route (min_via_grid 0.0001) (min_wire_grid 0.0001) (auto_fanout off) (auto_testpoint off) (auto_miter off)

Pre-Route the Tuff Stuff

- Since we have learned from experience that the auto-router is usually not effectively able to route some of the more difficult challenges such as, Diff Pairs orthogonal BUS routing, Zero via routing, etc…It is best to pre-route these kinds of nets/wires ahead of the lower priority, 'run-of-the-mill' wires/nets. Often a combination of auto and manual routing techniques can used together to efficiently complete the nets/wires that need to be pre-routed. Differential pairs are often good candidates for application of the auto/manual route completion technique. Below is a do file created specifically to route diff_pair nets.
  - ***Diff_pair route.do*** :
    tax via .3
    cost way 100
    unsel all routing
    select all pairs
    route 25
    clean 5
    route 50 16
    clean 5

tax via 1
cost way –1

Upon completion of the above .do file you will more than likely still need to complete and/or fine-tune some of your diff_pair nets. But hopefully the majority of them will be satisfactorily routed. Once you think the diff_pairs have been satisfactorily routed, you should protect them before proceeding with other routes.

- FSB (orthogonal) bus routing can sometimes also be completed with a combination of auto/manual routing. The process is:
    1. Select just the BUS nets for routing
    2. Smart-route them
    3. Evaluate results
    4. Manually finishing connect the wires *without* regard to length requirements
    5. Invoke the '***elong***' router
    6. Manually adjust the remaining wires to meet the length rule requirements
    7. Invoke the 'Miter' router to create the 45 degree bends
    8. Manually adjust wire lengths to meet remaining length violations
    9. Invoke, View => Visit => 90 Degree to find and eliminate all remaining 90 degree bends.
    10. Protect the completed, conflict free FSB nets.
    11. 11. Save a .rte file for to be used as starting pointing for potential future routing.

Other auto-routing tips and do files.

- Example of buried via auto-route do file:

```
Unselect all vias
Select BRVIASIG1_SIG2 BRVIASIG3_SIG4
select all nets
circuit selected (use_via  BRVIA-SIG1-SIG2 BRVIASIG3_SIG4 )
unsel all nets
tax way 1.5
tax via .3
route 25
clean 5
route 50 16
clean 5
route 100 16
clean 5
route 100 16
clean 5
```

Post-Route Considerations:

- Verify that the correct line widths were used. Especially for voltage nets.
- Run final checks (DRC report, dangling etch).