



Fig 1

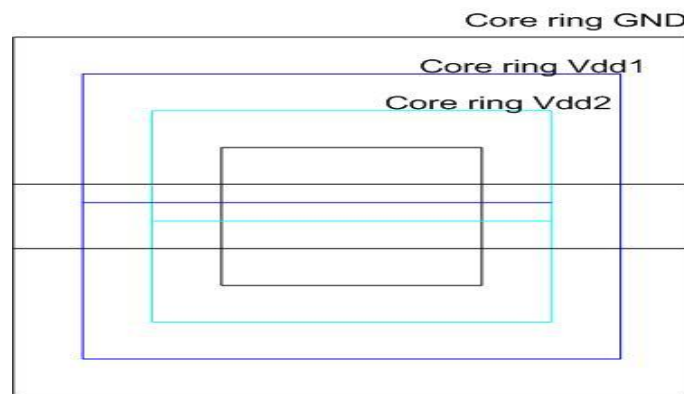


Fig 2

```

PIN vdd1[
    DIRECTION INOUT ;
    USE POWER ;
    SHAPE ABUTMENT ;
    PORT
        LAYER M1 ;
        RECT 0.000000 10.620000 5.040000 11.100000 ;
    END
END vdd1

PIN vdd2
    DIRECTION INOUT ;
    USE POWER ;
    SHAPE ABUTMENT ;
    PORT
        LAYER M1 ;
        RECT 0.000000 9.980000 5.040000 10.460000 ;
    END
END vdd2

PIN gnd
    DIRECTION INOUT ;
    USE GROUND ;
    SHAPE ABUTMENT ;
    PORT
        LAYER M1 ;
        RECT 0.000000 0.000000 5.040000 0.480000 ;
    END
END gnd

```

