

A complex digital circuit diagram for SAR logic, featuring multiple comparators, multiplexers, and control logic blocks interconnected on a grid background.

**SAR LOGIC**

A small circuit diagram of a Verilog comparator, showing two input lines and a single output line.

**Verilog  
comparator**

A circuit diagram for a DAC array, consisting of a regular grid of small, identical unit cells.

**DAC ARRAY**

A complex digital circuit diagram for SAR logic, similar to the top block, showing a dense arrangement of logic components.

**SAR LOGIC**

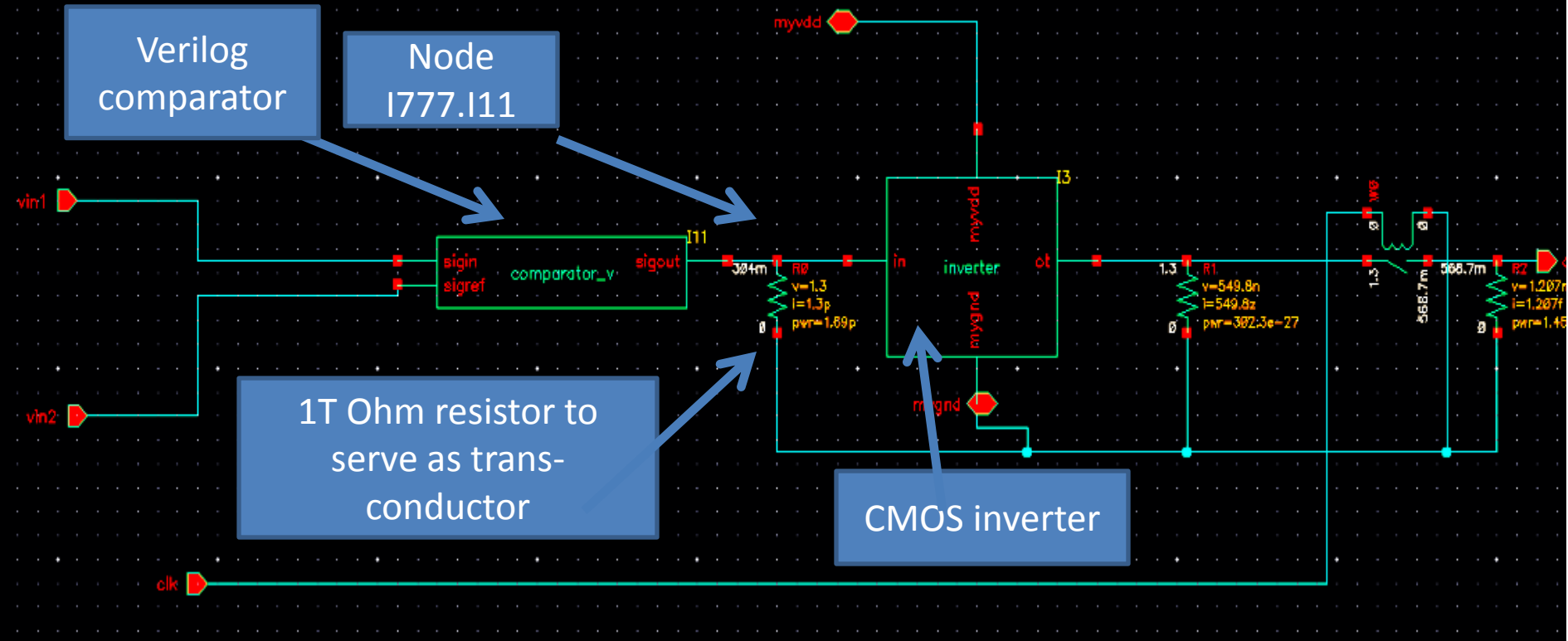
Verilog  
comparator

Node  
I777.I11

sigin  
sigref  
comparator\_v  
sigout

1T Ohm resistor to  
serve as trans-  
conductor

CMOS inverter



```
1777 (comparat_VW) Read veriloga
`include "discipline.h"
`include "constants.h"
module comparator( sign, sigref, sigout );
input sign, sigref;
output sigout;
electrical sign, sigref, sigout;
parameter real sigout_high = 1.3;
parameter real sigout_low = 0;
    analog begin
        if (V(sign) < V(sigref))    V(sigout) <+ sigout_low;
                                   if (V(sign) > V(sigref))    V(sigout) <+ sigout_high;
    end
endmodule
```

**This is a very simple comparator code.....and this results in convergence problem!!!! What should I change here????**

```
Created directory input.ahdlSimDB/2452_proj_65LPE_temp_sensor_comparator_v_veriloga_veriloga.va.comp
Created directory input.ahdlSimDB/2452_proj_65LPE_temp_sensor_comparator_v_veriloga_veriloga.va.comp
Compiling ahdlcmi module library.
Finished compilation in 1 s (elapsed).
Installed compiled interface for comparator.
```

```
Time for Elaboration: CPU = 133.979 ms, elapsed = 1.94945 s.
Time accumulated: CPU = 562.913 ms, elapsed = 2.45764 s.
Peak resident memory used = 103 Mbytes.
```

```
Time for EDB Visiting: CPU = 27.996 ms, elapsed = 28.198 ms.
Time accumulated: CPU = 590.909 ms, elapsed = 2.466 s.
Peak resident memory used = 104 Mbytes.
```

```
Notice from spectre during topology check.
```

```
No DC path from node `I1602.I18.net8' to ground, Gmin installed to provide path.
```

```
No DC path from node `I1602.I19.net8' to ground, Gmin installed to provide path.
```

```
No DC path from node `I1602.I22.net8' to ground, Gmin installed to provide path.
```

```
No DC path from node `I1602.I21.net8' to ground, Gmin installed to provide path.
```

```
No DC path from node `I1602.I23.net8' to ground, Gmin installed to provide path.
```

```
Further occurrences of this notice will be suppressed.
```

```
Warning from spectre during initial setup.
```

```
WARNING (SPECTRE-293): Too many saved signals [ 1147 ]. Slow initialization is expected!
```

```
Circuit inventory:
```

```
nodes 451
bjt 6
bsim4 834
capacitor 256
comparator 1
isource 2
relay 1
resistor 3
veri 13
vsource 17
```

This is not the problem off course!!

I am not sure about this

```

abstol(V) = 10 uV
abstol(I) = 100 pA
temp = 0 C
tnom = 27 C
tempeffects = all
errpreset = moderate
method = trap
literation = 3.5
relref = alllocal
cmin = 1 fF
gmin = 100 pS

```

My settings

This node is shown in  
Fig2\_comparator block

```

Notice from spectre at time = 4.03993 fs during transient analysis `tran'.
Maximum value for quantity `I' has increased to 417.619 mA (detected at I777.I11:sigout_flow).
Warning from spectre at time = 12.393 ps during transient analysis `tran'.
WARNING (SPECTRE-16191): Minimum time step used. Solution might be in error.
Notice from spectre at time = 12.393 ps during transient analysis `tran'.
Maximum value for quantity `I' has increased to 105.354 kA (detected at I777.I11:sigout_flow).
Warning from spectre at time = 12.393 ps during transient analysis `tran'.
WARNING (SPECTRE-16191): Minimum time step used. Solution might be in error.
Warning from spectre at time = 142.048 ns during transient analysis `tran'.
WARNING (SPECTRE-16191): Minimum time step used. Solution might be in error.
Warning from spectre at time = 142.048 ns during transient analysis `tran'.
WARNING (SPECTRE-16191): Minimum time step used. Solution might be in error.

```

```

tran: time = 2.497 us      (2.77 %), step = 338.7 ns      (376 m%)
tran: time = 7.68 us      (8.53 %), step = 1.8 us        (2 %)
tran: time = 11.28 us     (12.5 %), step = 1.8 us        (2 %)

```

```

Warning from spectre at time = 15.2425 us during transient analysis `tran'.
WARNING (SPECTRE-16191): Minimum time step used. Solution might be in error.
Further occurrences of this warning will be suppressed.
Warning from spectre at time = 15.2427 us during transient analysis `tran'.
WARNING (SPECTRE-16266): Error requirements were not satisfied because of convergence difficulties.

```

```

tran: time = 15.76 us     (17.5 %), step = 232 ns        (258 m%)
tran: time = 20.27 us     (22.5 %), step = 35.14 ns      (39 m%)
tran: time = 25.58 us     (28.4 %), step = 1.415 us      (1.57 %)
tran: time = 29.32 us     (32.6 %), step = 160 ns        (178 m%)
tran: time = 33.78 us     (37.5 %), step = 238.3 ns      (265 m%)
tran: time = 38.52 us     (42.8 %), step = 528.7 ns      (587 m%)
tran: time = 43.02 us     (47.8 %), step = 502.5 ns      (558 m%)
tran: time = 47.27 us     (52.5 %), step = 123.7 ns      (137 m%)
tran: time = 51.75 us     (57.5 %), step = 248.4 ns      (276 m%)
tran: time = 56.36 us     (62.6 %), step = 358.6 ns      (398 m%)
tran: time = 61.01 us     (67.8 %), step = 293.1 ns      (326 m%)
tran: time = 65.25 us     (72.5 %), step = 13.48 ns      (15 m%)

```

Red lines show the  
convergence  
problems spectre is  
facing!!!!